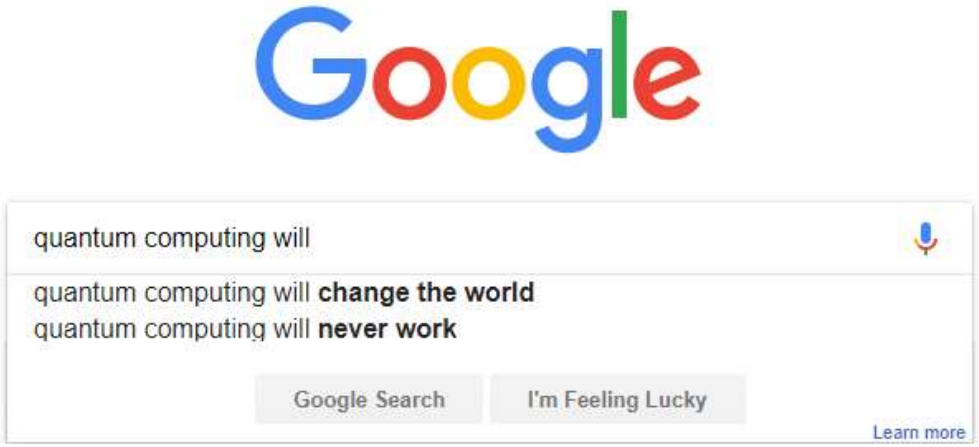
SI MOS SPIN QUBITS FOR QUANTUM COMPUTING

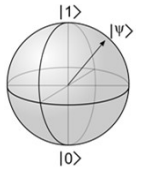
Louis Hutin – louis.hutin@cea.fr | July 9 2019

WHAT WILL QUANTUM COMPUTING DO?

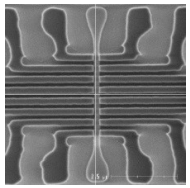


OUTLINE

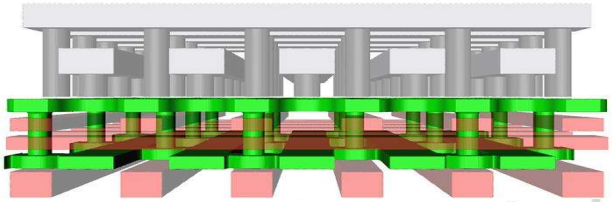
1 Quantum computing and Si spin qubits



2 Linear arrays of Si MOS quantum dots



3 Higher dimensional architectures for fault-tolerant QC



4 Perspectives for scaling up

CLASSICAL BIT VS. QUANTUM BIT

A classical bit can be a vector pointing either to 1 or 0.

CLASSICAL BIT VS. QUANTUM BIT

State described as a **superposition** of two basis states, with a **phase** term between their coefficients.

$$|\psi\rangle = cos\frac{\theta}{2}|0\rangle + e^{i\varphi}sin\frac{\theta}{2}|1\rangle$$

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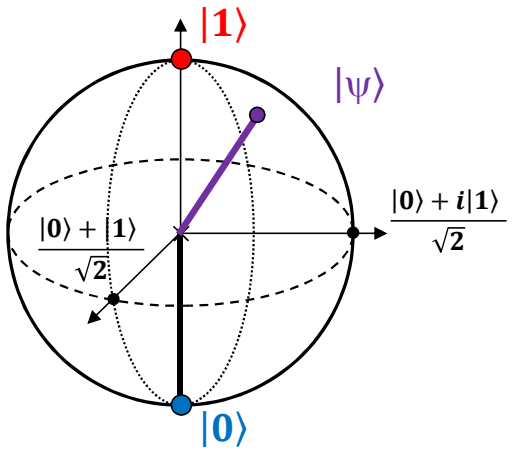

A quantum bit can point to anywhere on this unit sphere.

CLASSICAL BIT VS. QUANTUM BIT

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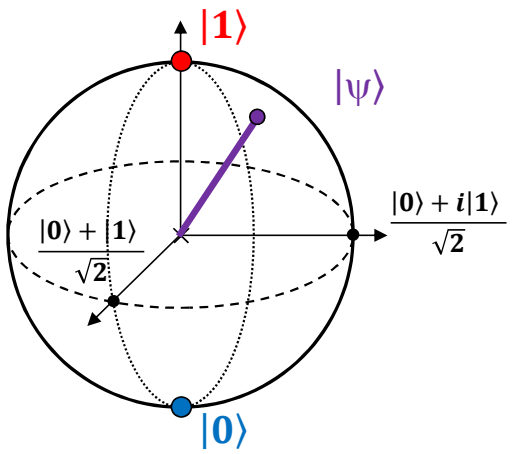
$$|\psi\rangle = cos\frac{\theta}{2}|0\rangle + e^{i\varphi}sin\frac{\theta}{2}|1\rangle$$

This is precisely how **two-level quantum systems** behave:

- polarization of a photon
- ***spin of an electron***/atom/molecule
- electronic states of a trapped ion
- presence or absence of a charge in a quantum dot
- modes of a superconducting / nanomechanical oscillator
- …



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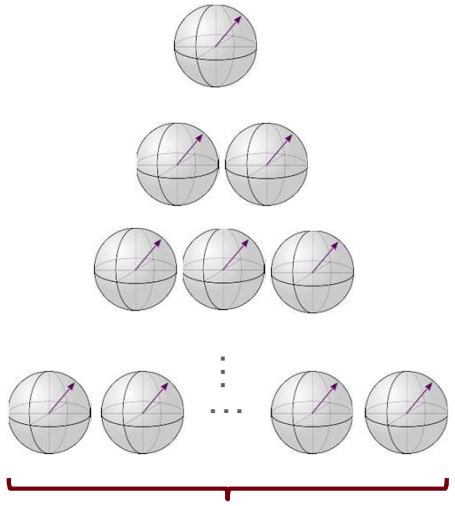
QUANTUM PARALLELISM

- **1 op onto N basis states = N ops simultaneously**
- **Adding 1 qubit multiplies the number of basis states by 2**



N (entangled) qubits

$$|0\rangle + |1\rangle \xrightarrow{\boxed{f}} f(|0\rangle) + f(|1\rangle)$$

$$|00\rangle + |01\rangle + |10\rangle + |11\rangle \xrightarrow{\boxed{f}}$$

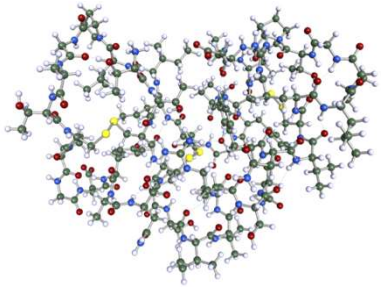
$$|000\rangle + |001\rangle + |010\rangle + |011\rangle + |100\rangle + |101\rangle + |110\rangle + |111\rangle \xrightarrow{\boxed{f}}$$

… calculation on a superposition of 2^N basis states.

30 qubits: 10^9 operations in parallel

300 qubits: 10^{90} (>nb of atoms in the universe)

HOW MANY QUBITS DO WE NEED?



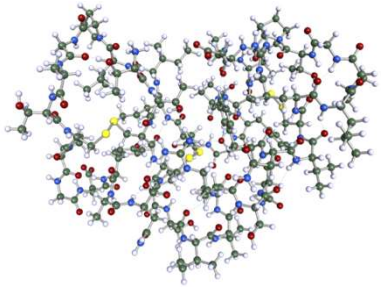
Quantum chemistry for **medicine** and **material development:**
>200 logical qubits

Prime factorization of large numbers for **security**:
>2000 logical qubits

Quantum supremacy in **simulation**:
>56 logical qubits

HOW MANY QUBITS DO WE NEED?

Redundancy for Quantum Error Correction!



Prime factorization of large numbers for **security**:
>2000*1e3-1e5 qubits

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Quantum supremacy in **simulation**:
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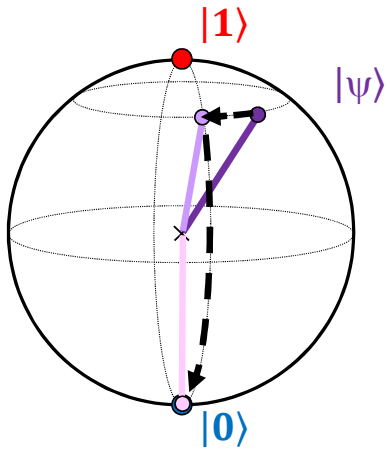
At least a million:
Qubit platform needs to be **extensible.**

QUANTUM INFORMATION IS FRAGILE



Interactions with **noisy environment** will cause errors (decoherence) due to:

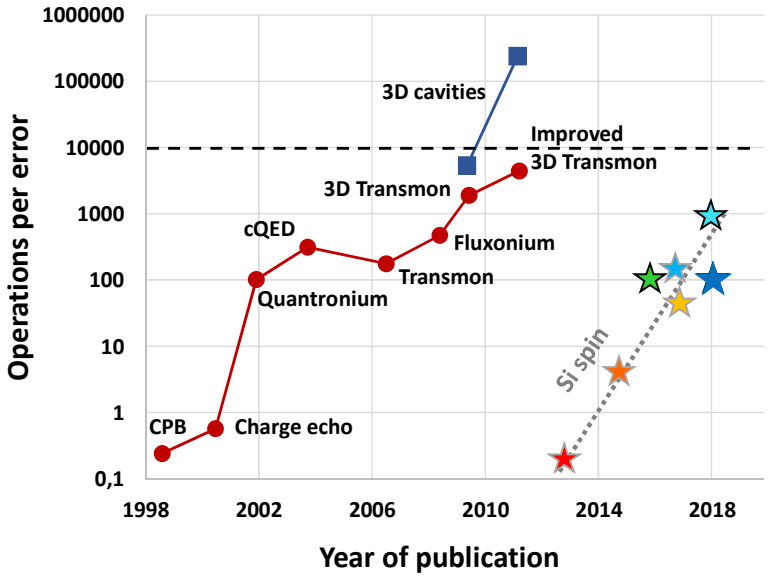
- **Dephasing**
- **Relaxation**

Qubits defined in the **best-isolated systems have the longest coherence times**… they are also **harder to manipulate (slow)**.

Q-factor: number of rotations in the sphere before losing coherence.
Measure of the **stability/addressability trade-off**

SI QUBITS: LATE BUT ON THE RISE

- **Excellent outlook on extensibility** due to small size and compatibility w/ VLSI techniques.
- **Material engineering** (isotopic purification, charge noise reduction…) **and control schemes** development have kept the **Q-factor increasing**.

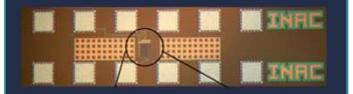


- Yoneda *et al. (RIKEN), Nature Nano 2018*: Quantum dot electron spin qubit in ^{28}Si/SiGe
- Takeda *et al. (RIKEN), Science Adv. 2016*: Quantum dot electron spin qubit in ^{nat}Si/SiGe
- Zajac *et al. (Princeton), Science 2018*: Quantum dot electron spin qubit in ^{nat}Si/SiGe
- Veldhorst *et al. (UNSW), Nature 2015*: Quantum dot electron spin qubit in ^{28}Si
- Maurand *et al. (CEA), Nature Comm. 2016*: CMOS hole spin qubit in natural Si
- Kawakami *et al. (TUDelft), Nature Nano 2014:* Quantum dot electron spin qubit in ^{nat}Si/SiGe
- Pla *et al. (UNSW), Nature 2012*: Single-donor electron-spin qubit in natural Si

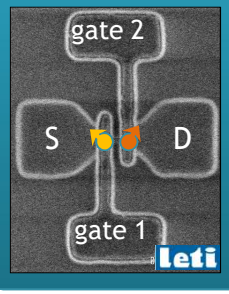
A COMMON TECHNOLOGY PLATFORM

Si CMOS technology
FDSOI

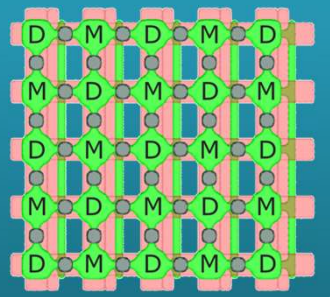
Cryogenic peripheral electronics



Spin qubit devices



Large-scale qubit integration



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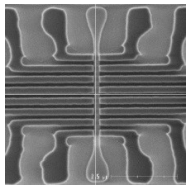


2 **Linear arrays of Si MOS Quantum Dots**

3 Higher dimensional architectures for fault-tolerant QC

4 Perspectives for scaling up

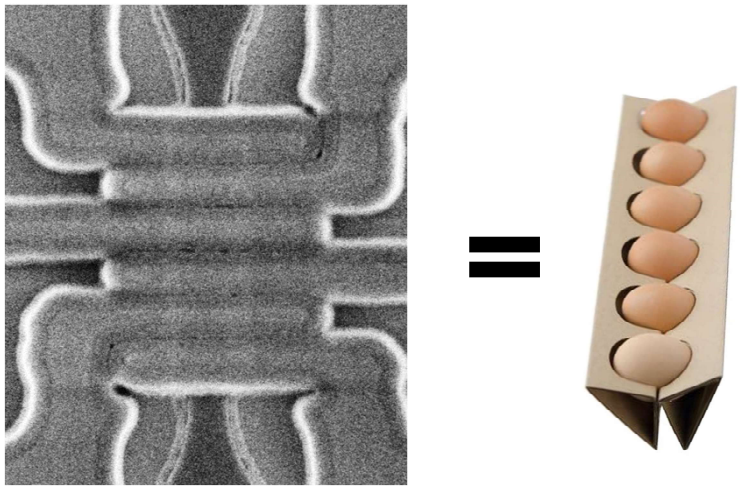
STEP 1: CHARGE CONFINEMENT

To make a N-qubit register:

- confine N electrons
- possibility of nearest neighbor coupling

⇒ Use MOS Gates on a SOI NanoWire to form a Coulombian « egg-carton »

⇒ Load electrons (eggs) from the side reservoirs



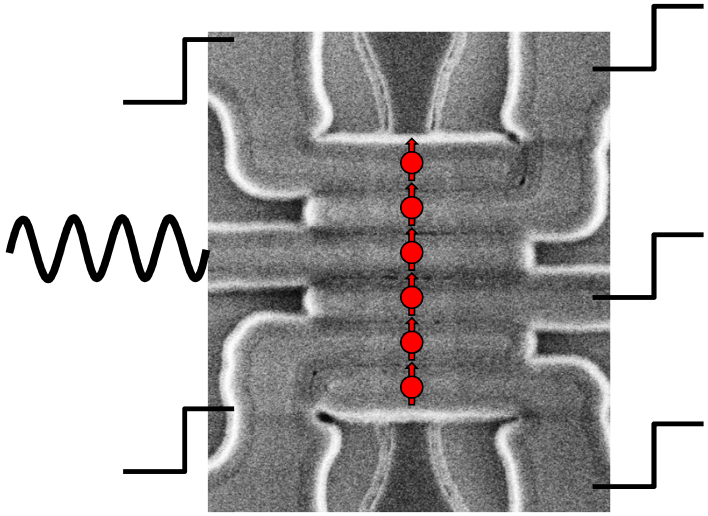
STEP 2: SPIN MANIPULATION

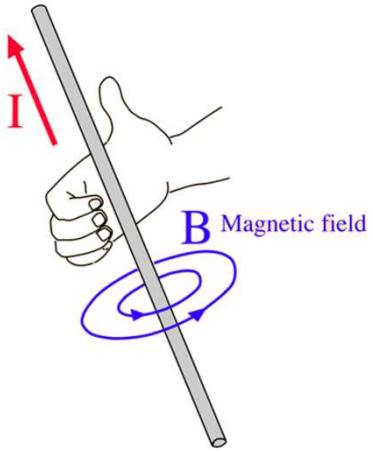
To induce spin transitions:

- Provide MW excitation at the spin resonance frequency

⇒ May be applied locally by E-Field on Gates (fast but unstable)

⇒ May be applied globally by B-Field, E-Field used on Gates to tune qubit in/out of resonance (stable but slow)

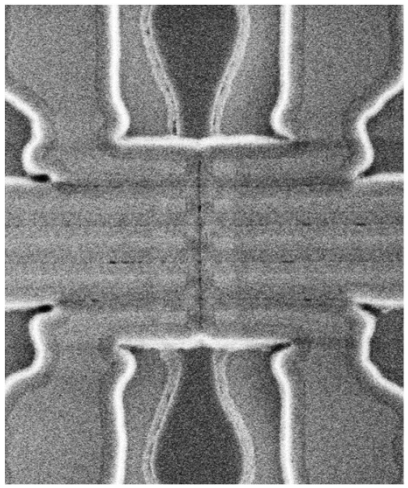




STEP 3: SPIN READOUT

To sense a spin event:

- Implement spin-to-charge conversion scheme
- Use a neighboring sensor (also a Quantum Dot)



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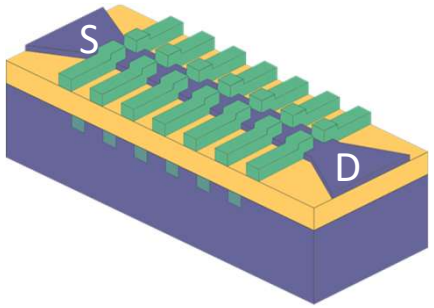
DERIVATIVE APPROACH: TEST VEHICLE



Fast prototyping - obvious CMOS-compatibility
Limited qubit interconnectivity

- Has enabled so far:

All-electrical hole spin qubit
R. Maurand et al., Nature Communications, 2016
L. Hutin et al., VLSI 2016

All-electrical electron spin manipulation
A. Corna et al., npj Quantum information, 2018

Tunable spin-valley mixing using SOI backgate
L. Hutin et al., VLSI 2018
L. Bourdet et al., Phys Rev. B, 2018

Single-shot spin readout
M. Urdampilleta et al., VLSI 2017
A. Crippa et al., Nature Communications, 2019
M. Urdampilleta et al., Nature Nanotechnology, 2019

- Will keep teaching us:

- Impact of materials on decoherence (dielectrics, interfaces, ^{28}Si…)
- Q-factor optimization
- High-fidelity measurements
- Long range coupling strategies
- …

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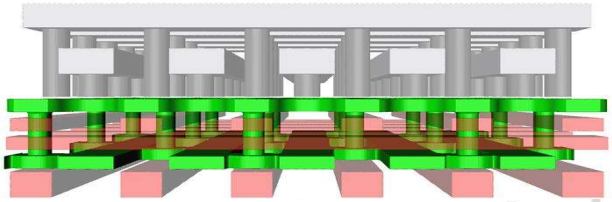
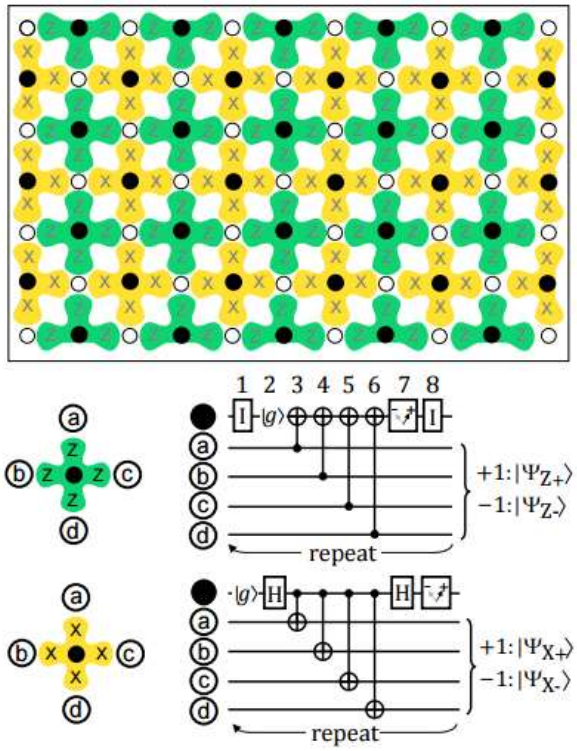


4 Perspectives for scaling up

SURFACE CODE IN A 2D ARRAY



A. G. Fowler *et al.*,
Phys. Rev. A 86, 2012

Surface code is popular b/c compatible with 1% error threshold (⇔ **Q>100**)

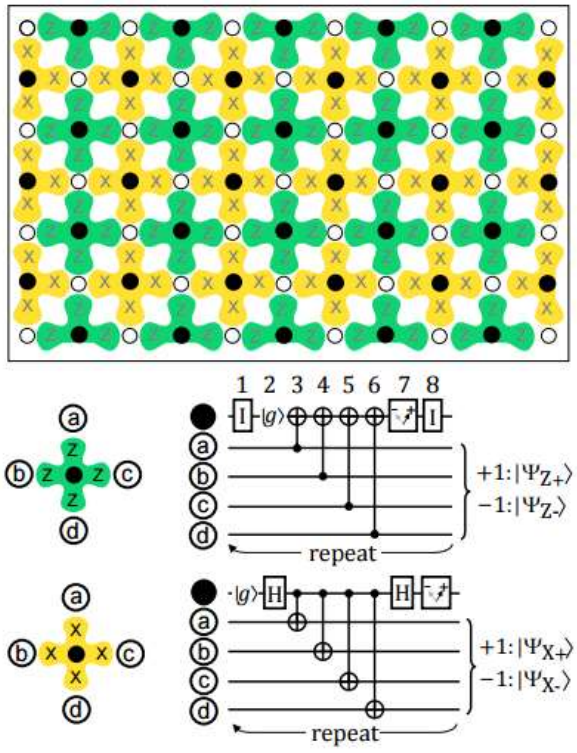
It takes a minimum of thirteen physical qubits to implement a single logical qubit. A reasonably fault-tolerant logical qubit that can be used effectively in a surface code takes of order 10^3 to 10^4 physical qubits.[1]

[1] This number depends strongly on the rate that errors occur on the physical qubits.

Not compatible w/ traditional MOS layout

⇒ **Custom integration of 2D Quantum Dot arrays**

SURFACE CODE IN A 2D ARRAY



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Each physical qubit should be individually addressable

Where do we fit:

- Qubit readout (charge detectors)?
- Addressing classical transistors?

Can we handle:

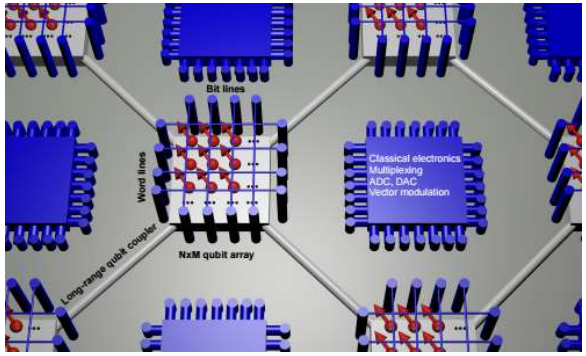
- Crosstalk (cf. fidelity)?
- Data rates of refreshed readout?
- Power dissipation?

HYBRID CIRCUITS, 3D STACKING

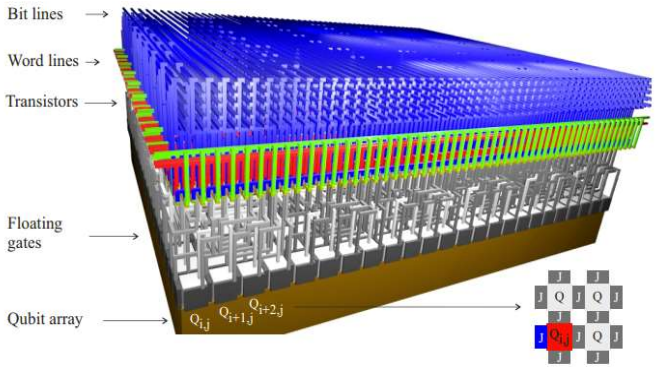
HYBRID CIRCUITS

- Monolithic coplanar integration of classical and quantum electronics

⇒ **Requires long-range qubits coupling**



L.M.K. Vandersypen *et al., npj Quant. Inf.* (2017)



M. Veldhorst *et al. (UNSW), Nature Comm.* (2017)

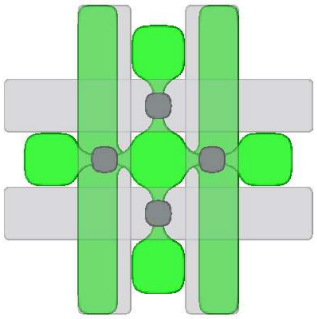
3D STACKING

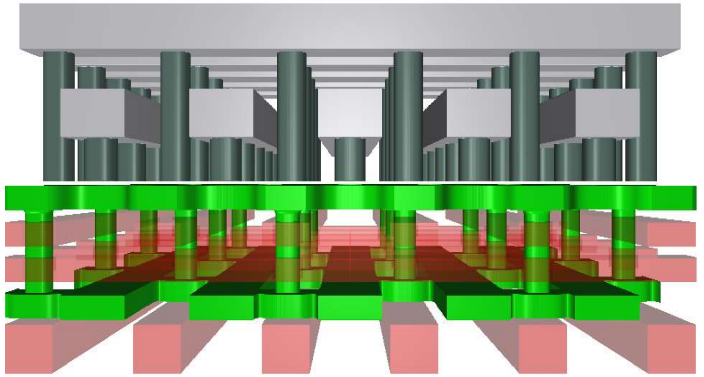
- Requires two or more superimposed active layers
- Very high density of vias and interconnects

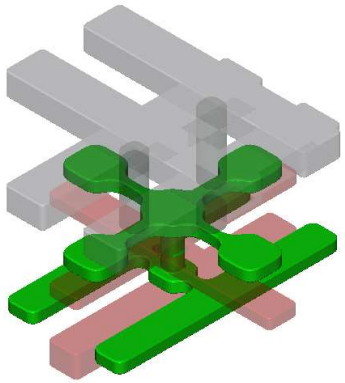
⇒ **Challenges: alignment, managing cross-talk**

⇒ **CoolCube™ expertise in Leti**

EXTENSIBLE ARCHITECTURES FOR FAULT-TOLERANT QC







T. Meunier *et al. (CNRS), VLSI 2019*

- **Several groups (UNSW, QuTech / Intel, CEA/CNRS)** thinking about large 2D (or 3D) arrays of QDs.
- Convergence on **crossbar addressing** due to I/Os bottleneck
- Different stances on **balancing density, cross-talk and variability** management
- Strong local partnership around ERC Synergy project QuCube (Leti/IRIG/CNRS I-Néel)

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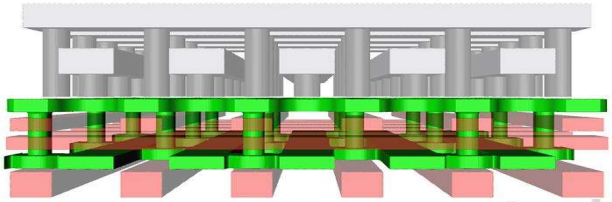


4 **Perspectives for scaling up**

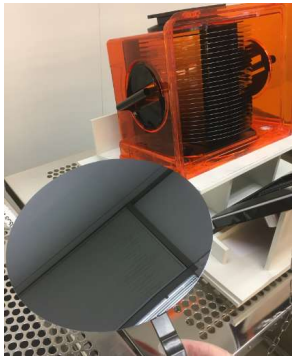
HOT TOPICS FOR COLD QUBITS: ^{28}SI

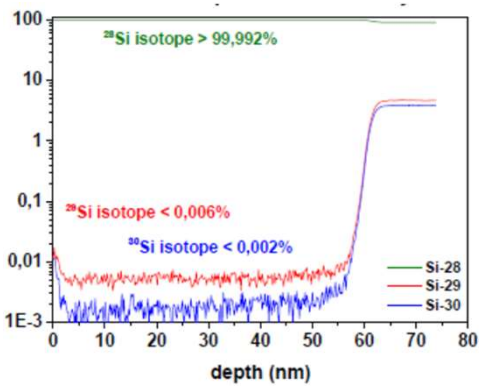
Coherence time will set a limit to how large a qubit array can be.

^{28}Si is nuclear spin-free (^{29}Si is not): improved coherence

- Collaboration with the Russian Academy of Sciences: conversion of ultra-centrifuged $^{28}SiF_4$ into $^{28}SiH_4$

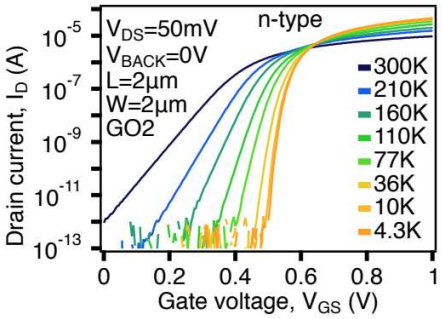
- Silane-based epitaxial growth onto **300mm** wafers at Leti with **99.992% purity** and high uniformity.

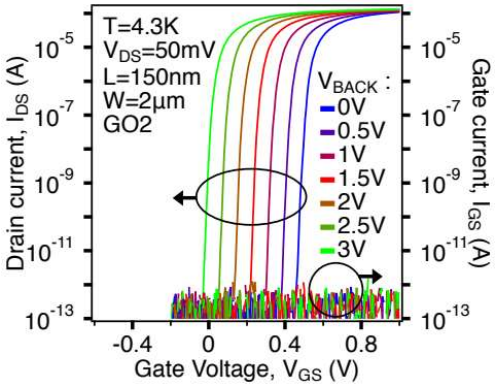




V. Mazzocchi et al., J. Crystal Growth, 509, 2019

HOT TOPICS FOR COLD QUBITS: CRYO-CMOS





H. Bohuslavskyi et al., IEEE TED 2018

FDSOI for on-chip control electronics

- Power dissipation constraints warrant low supply voltage operation.
- The subthreshold slope steepens at very low T, which may be good or bad.
- **The ability to shift the whole MOSFET characteristics with a back-Gate bias and no channel doping is an important design asset.**
- **FDSOI also a local specialty.**

HOT TOPICS FOR COLD QUBITS: LONG RANGE COUPLING

Use **MW photons in co-integrated superconducting resonators** to couple distant Si spin qubits.

Science

QuTech - 25/01/2018

Strong spin-photon coupling in silicon

N. Samkharadze,[1*] G. Zheng,[1*] N. Kalhor,[1] D. Brousse,[2] A. Sammak,[2] U. C. Mendes,[3] A. Blais,[3,4] G. Scappucci,[1] L. M. K. Vandersypen[1†]

[1]QuTech and Kavli Institute of Nanoscience, Delft University of Technology Lorentzweg 1, 2628 CJ Delft, Netherlands. [2]QuTech and Netherlands Organization for Applied Scientific Research (TNO), Stieltjesweg 1 2628 CK Delft, Netherlands. [3]Institut Quantique and Département de Physique, Université de Sherbrooke, Sherbrooke, Québec J1K 2R1, Canada. [4]Canadian Institute for Advanced Research, Toronto, Ontario, Canada.

10.1126/science.aar4054 (2018)

Princeton - 14/02/2018

nature
International journal of science

A coherent spin–photon interface in silicon

X. Mi[1], M. Benito[2], S. Putz[1], D. M. Zajac[1], J. M. Taylor[3], Guido Burkard[2] & J. R. Petta[1]

doi:10.1038/nature25769

GENERAL CONCLUSIONS

- Quantum information is very **powerful, yet fragile**. For each possible qubit platform: **stability/addressability/extensibility trade-off**.
- Quantum technologies are still at an **early stage**. Particularly true for **Si spin qubits**, not the leading approach but on the rise, with **high potential for extensibility**.
- SOI NW transistor geometry still a useful learning vehicle, but topological compatibility with **QEC will require dedicated 3D** QD array designs and integration schemes.
- The challenges to be met for quantum hardware alone are important. In this case and for fault-tolerant architectures: **material engineering, high density 3D integration, dissipation / cross-talk / data rates management**.

- **Plenty of opportunities for innovation!**

Thank you!

Scott Adams/Dilbert

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www.leti-cea.com