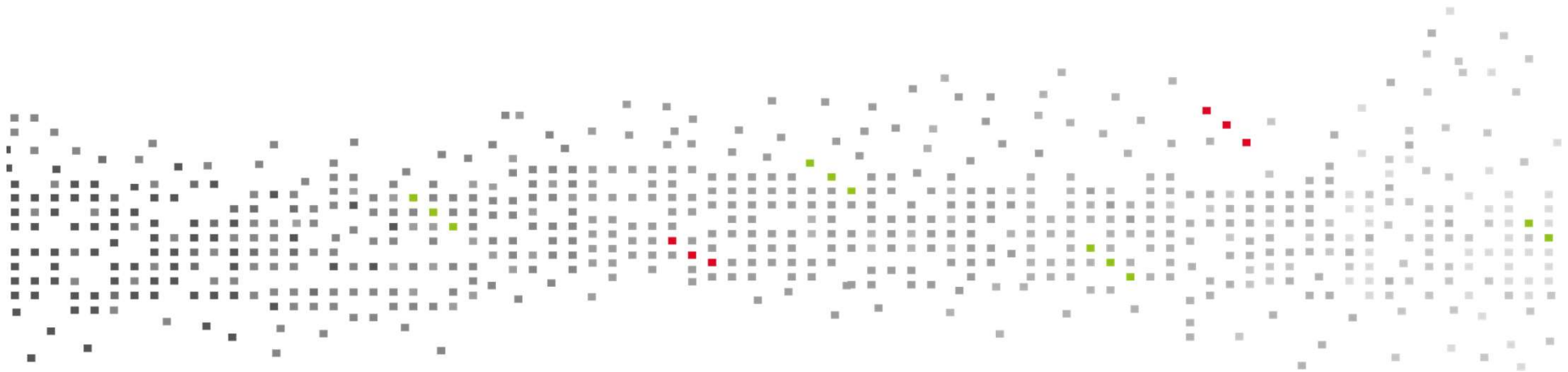


**leti**  
cea tech



## TECHNOLOGY PLATFORM : OUTLOOK & CAPABILITY

SEMICONWEST 2019 - FRAUNHOFER LETI WORKSHOP

July 2019 | L CLAVELIER - L PAIN

# ABOUT THE MICRO, NANO-ELECTRONICS & PHOTONICS PLATFORMS

## 300mm & 200mm Si components Platforms

- ~270@200mm equipments
- ~105@300mm equipments
- 5600 square meters Cleanroom - ISO3-5
- 24/7 operations

## 200mm MEMS Platform

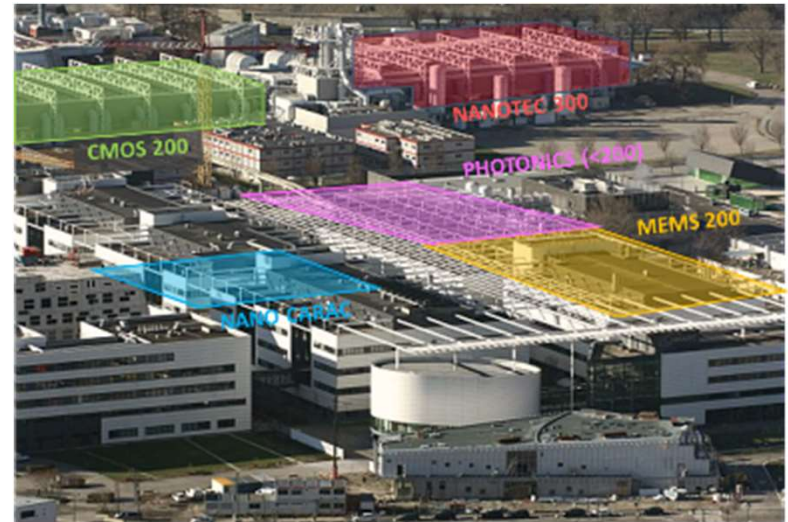
- ~130@200 mm equipments
- 2200 square meters - ISO 4-5
- 24/7 operations

## Substrates <200 mm, III-V and II-VI Platform

- ~230 @ various diameter equipments
- 1000+1000 square meters - ISO 4-5
- 1shift/day

## Nano-CHARACTERIZATION Platform

- ~ 40 huge equipments
- 2200 square meters
- 8 centers of competences



## PLATFORM ID CARD :

- >700 equipments on 10000m<sup>2</sup> of clean room >500 talented people including **international experts**
- >150 scientific papers published in 2018
- ~40 patents filed in 2018
- 7/24 operations



# OUR COLLABORATION OFFER



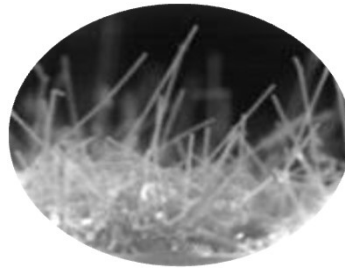
## New products & applications

- Collaboration thru LETI's Silicon Product Divisions (DCOS, DOPT, DTBS)



## Mature Processes & Technologies

- Wafer service thru LETI 3S (Silicon Specialties Solutions)
- IP licensing
- Technology Transfer



## New Materials & Process Development

- Collaborative bilateral research on specific project
- Common laboratories
- Affiliation program



## New Equipment Engineering

- Specific Joint Development Program

**A full range of business models to meet our partner's needs**

## <200mm, 200mm & 300mm PLATFORMS

### < 200mm

1. II-VI material
2. II-VI components
3. III-V material
4. III-V components
5. X-OI substrates

### 200mm

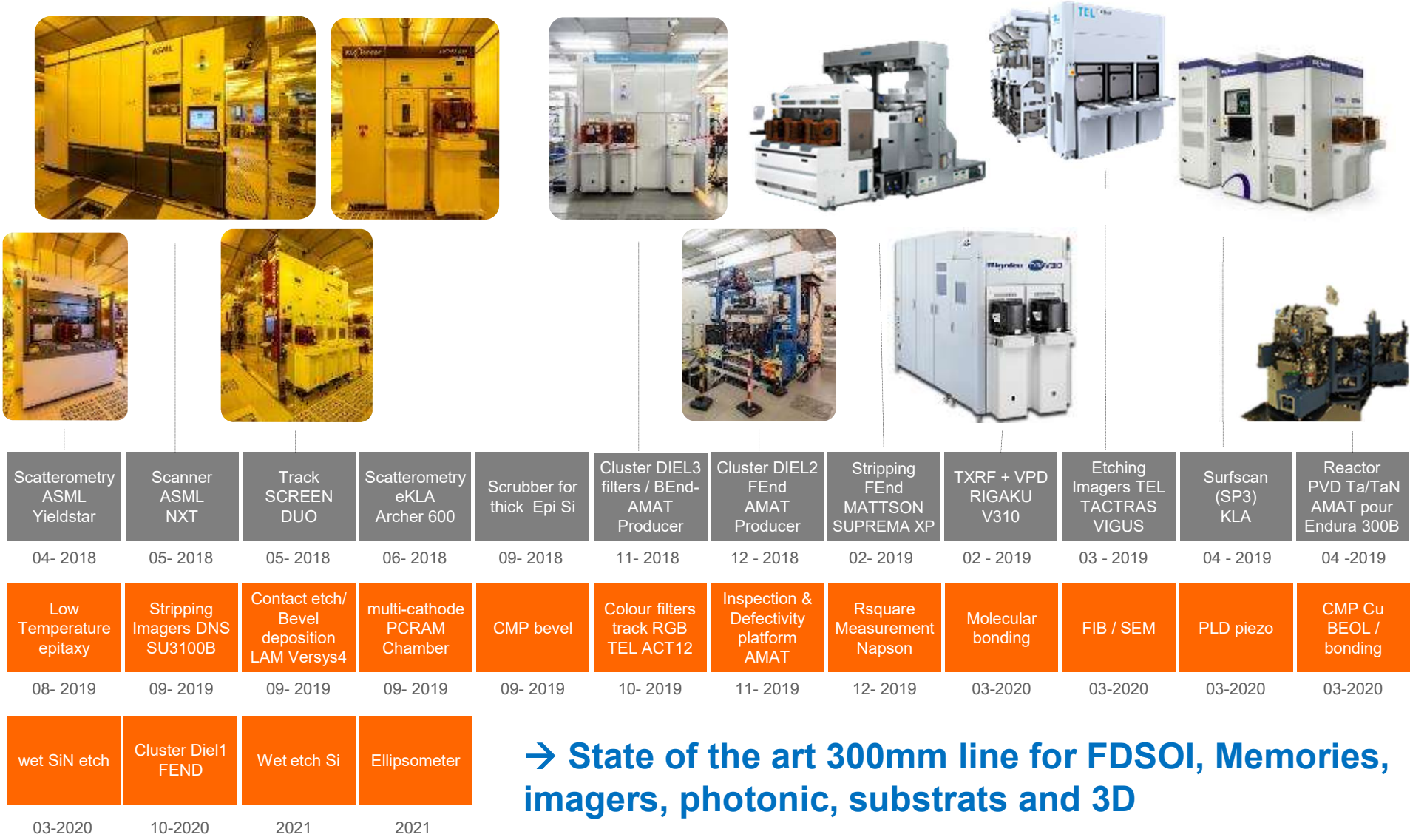
1. Power GaN and RF
2. Sensor
3. Display
4. Lighting
5. Photonic on Si
6. 3D Integration
7. SOI substrates

### 300mm

1. Imager
2.  $\mu$ Controller/eNVM
3. Photonic on Si
4. 3D Integration
5. FDSOI & Quantum
6. SOI substrates



# EVOLUTION OF THE 300mm TOOL SET

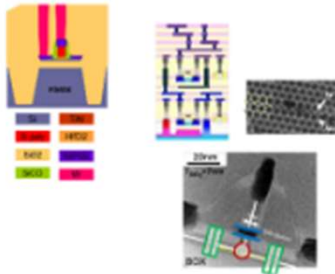


→ State of the art 300mm line for FDSOI, Memories, imagers, photonic, substrats and 3D

# 6 technological roads available in 300mm and more

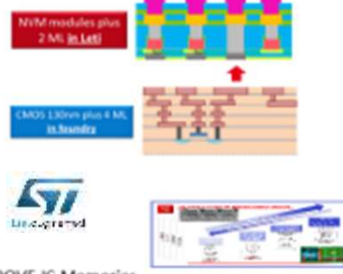
## Advanced Nano-Elec 300mm ROADS

### FDSOI – BEYOND CMOS



- Computing, low power, coolcube, ...
- 120 process step flow (short version)
- 8 levels of litho (and more)
- C28 compatible and lower

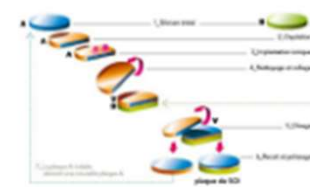
### MEMORIES



- ABOVE IC Memories
  - OXRAM
  - PCRAM
- 120 process step flow
- 9 levels of litho
- C28 compatible and lower

## Enablers

### SOI SUBSTRATES



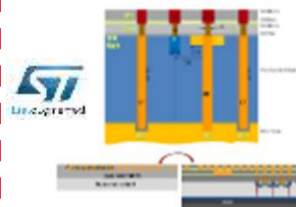
soitec



- RFSOI, Imager SOI, Photonic/Power SOI, FDSOI
- 30 process step flow
- Prototyping capability

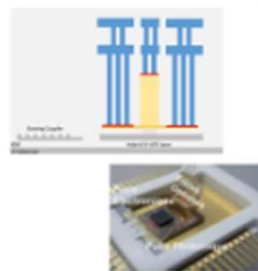
## OPTO 300mm ROADS

### VERTICAL IMAGERS



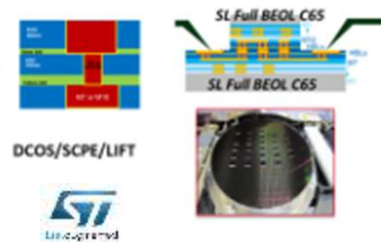
- Full CMOS compatible process
- Long range 3D imagers
- 120 process step flow
- 9 levels of litho

### PHOTONIC

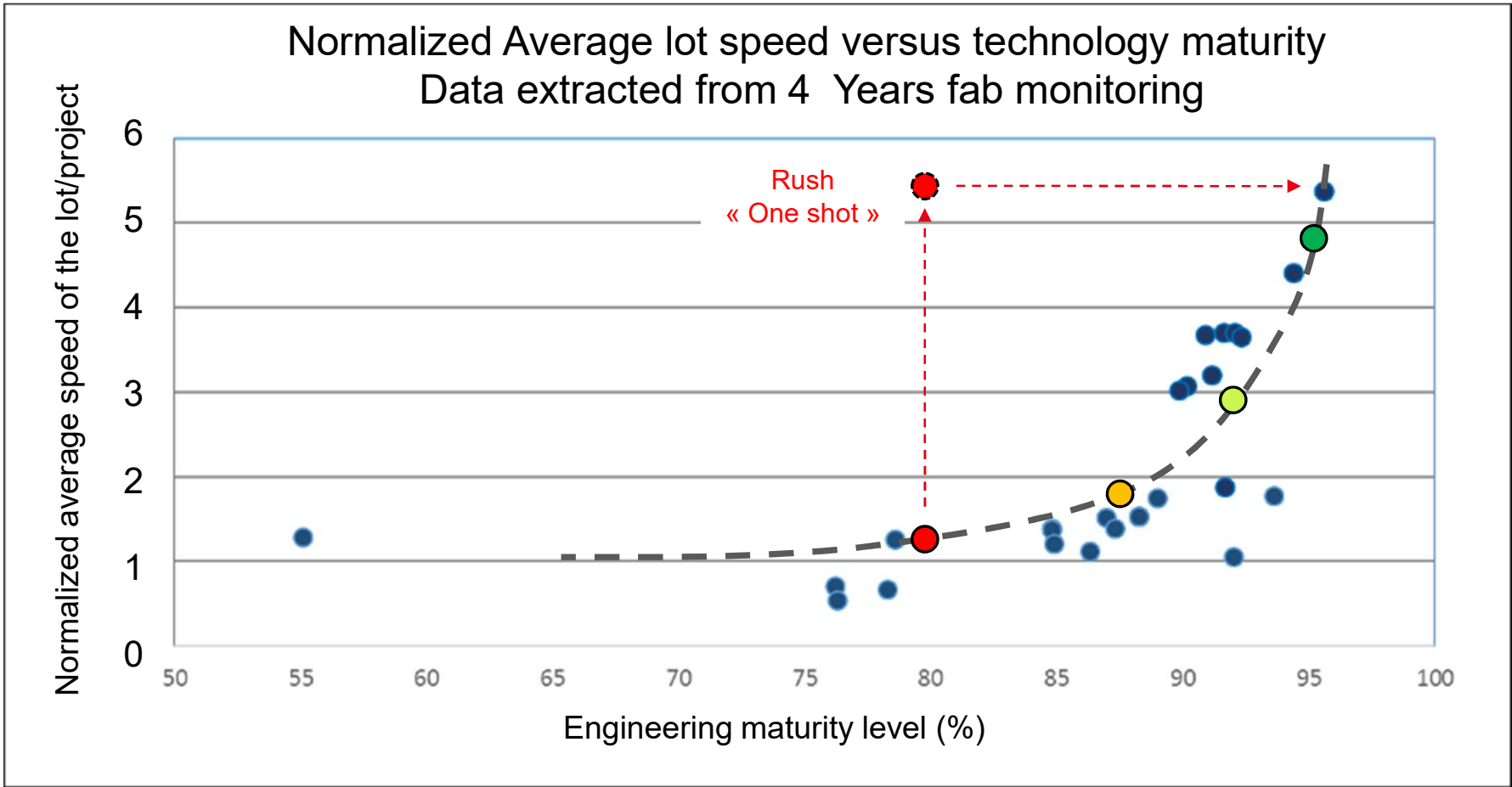


- Passive (WG, switches, ...) and active (III-V)
- full CMOS compatible process
- Communication and HPC
- 150 process step flow
- 15 levels of litho

### 3D

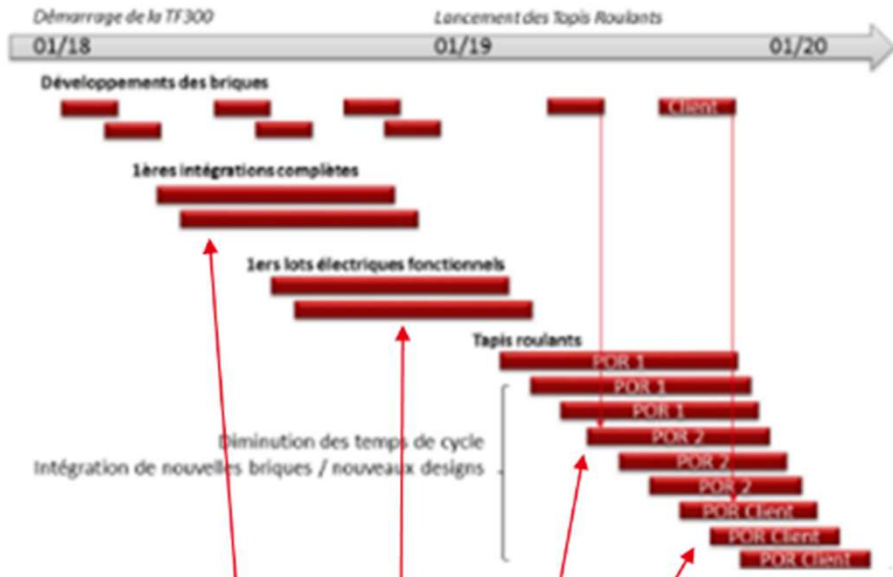


- Interposer, 3D SoC (→ computing, displays,...)
  - Hybrid bonding Cu-Ox
  - TSV 1:12 – 1:15
- 60 process step flow
- 4 levels of litho
- W2W (and C2W)

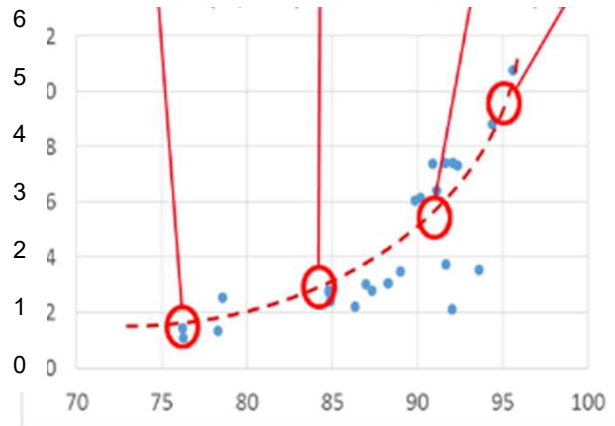


*Data measured on more than 400 lots -Year 2018*

# PERFORMANCE PLAN RAMP UP 2018-2020 RECURRENT BATCH LAUNCH ON STABILIZED FLOWS



Lot speed (step/week) vs normalized maturity (%)



Engineering maturity level (%)

**Strengths of Recurrent batches**

- Reduced engineering / lot (Eng mat > 93%)
- More lots with POR in WIP
- Reduced process steps (In line control)
- Improved cycle time

**Experienced on FDSOI : it works !**

**Approach compatible for fast R&D cycle time**

**Already validated**  
→ FDSOI baseline

**Strategy deployed in 2019 on**  
→ Photonic  
→ Power device  
→ Substrate  
**Other to come in 2020**



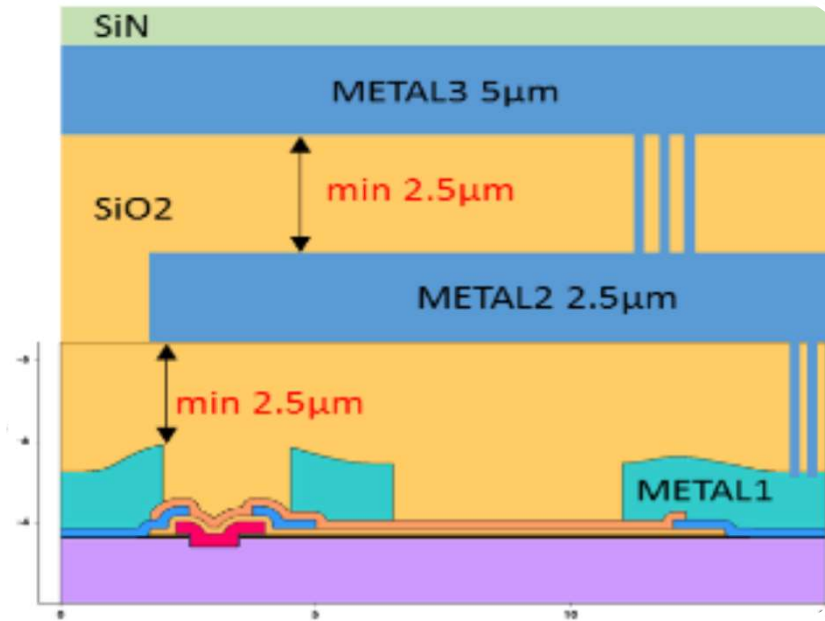


# 200mm GaN : POWER DEVICES



September  
24<sup>th</sup>  
2018

## Base Line for GaN/Si MOS and Diodes



## ST and Leti to make GaN-on-Si power transistors

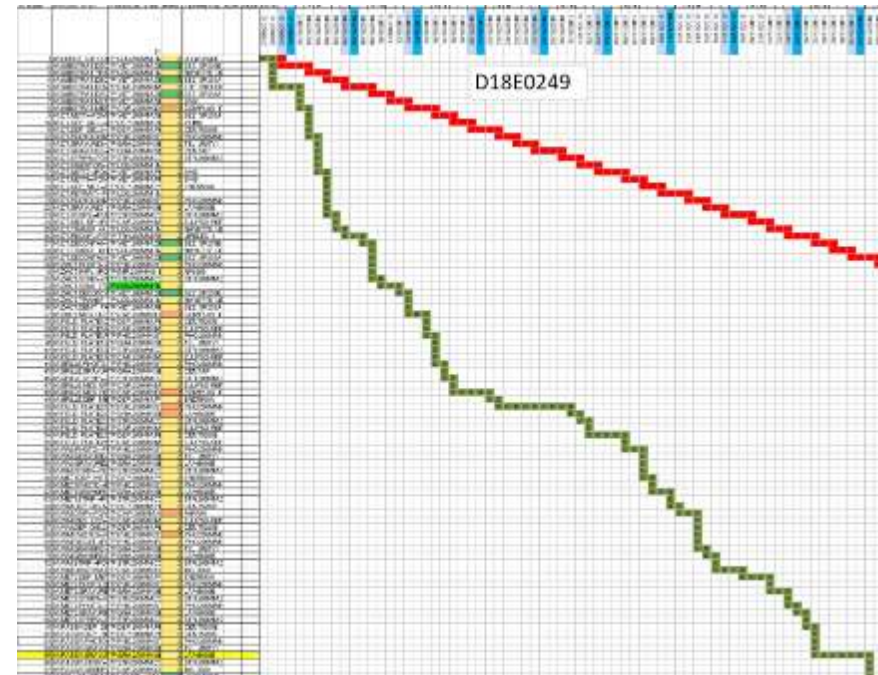
STMicroelectronics to manufacture GaN-on-Si power transistors, based on a process developed by French research lab [Leti](#), ST and IRT Nanoelec.



The process will be transferred from Leti's 200mm R&D line to an ST-operated 200mm-wafer pilot-line, operational by 2020, which will allow IRT to address high-efficiency high-



## POWER-GaN base line example with ST



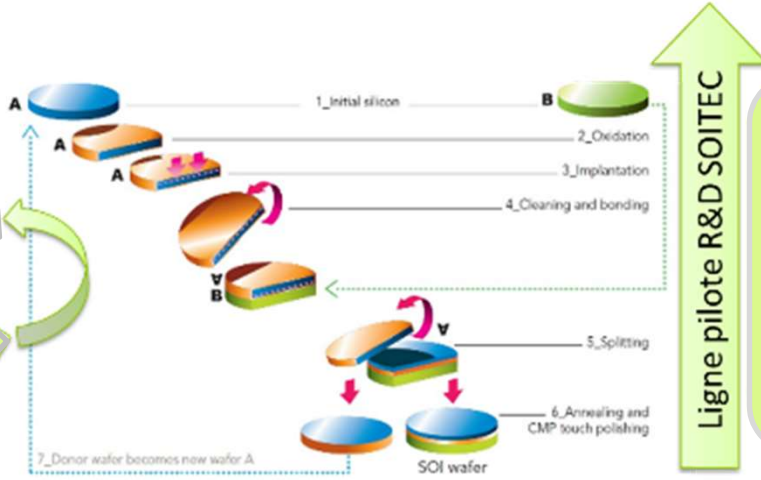
**10 step/w in average → 9-10 week cycle time  
with recurrent batches approach implemented  
Full compatible with MPW approach**



# 100-300mm SUBSTRATES PROTOTYPING LINE WITH SOITEC



**R&D comon lab**  
 Derivatives techno blocks  
 Epitaxy trap rich :  
 Functionalization  
 Thick top Si  
 Thick BOX bonding  
 Disruptive finishing  
 & uniformities



**Ligne pilote R&D SOITEC**

- 1 – R&D technology modules validation
- 2 – Prototyping possibility
- 3 – Acceleration & transfer to SOITEC for large scale ramp up

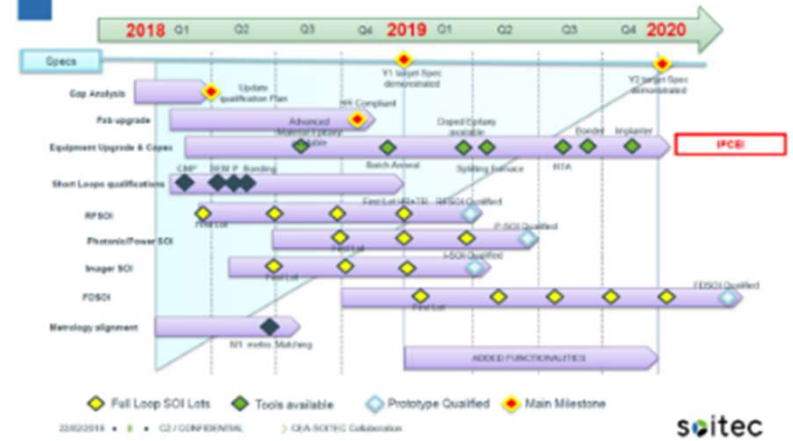


## 30033 SOI equipments localization



CONFIDENTIEL

## R&D Pilot Line Chart and Milestones (Soitec Request)



CONFIDENTIEL



# A WORLDWIDE ECOSYSTEM FOR COMPONENTS MANUFACTURING



Equipment



Electronics



Energy

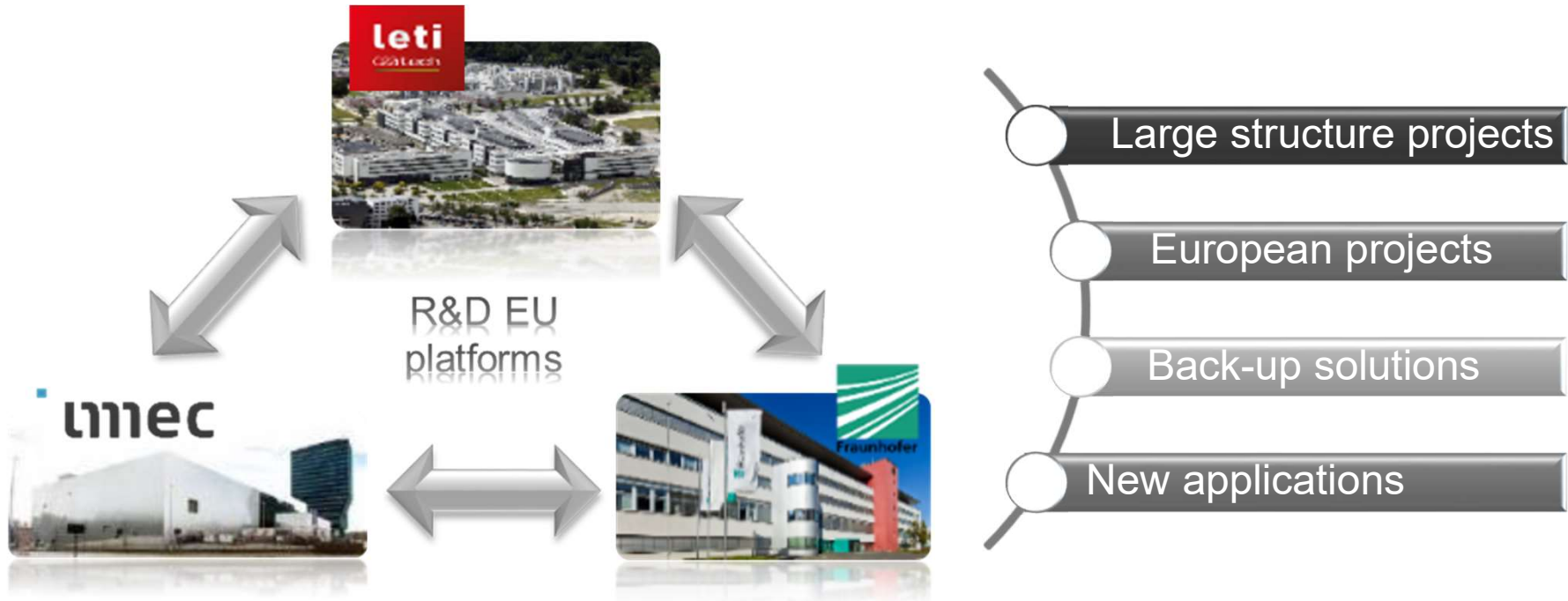


Communication

5G, RF



# A COMPLETE SYNERGIE AT EUROPEAN LEVEL



- State of the art 100-200-300mm tool set & technologies in « one stop shop »
- From R&D to Industrial Transfer thanks to Highly skilled teams coming from both worlds
- Full compatible with all Fab requirements (flying wafers)
- Access to the SOITEC-CEA « substrate innovation center »
- Access to
  - Specific device developments for your needs
  - or
  - Access to our recurrent batches (MPW, tool and material assessment)
    - FDSOI CMOS and cool cube
    - R-RAM memories
    - GaN power devices
    - Substrates (Substrate Innovation Center)
    - III-V photonic on Si
    - 3D
    - ...
- Confidentiality management & IP protection