NAAICE
Network-Attached Accelerators in Heterogeneous Computing Environments

Fraunhofer-Institut für Nachrichtentechnik Heinrich-Hertz-Institut Berlin, Helmholtz-Zentrum Potsdam Deutsches GeoForschungsZentrum, PERFACCT Performance Acceleration Technologies GmbH, Universität Potsdam, Zuse-Institut Berlin

1 NAAICE Project Objectives and Goals

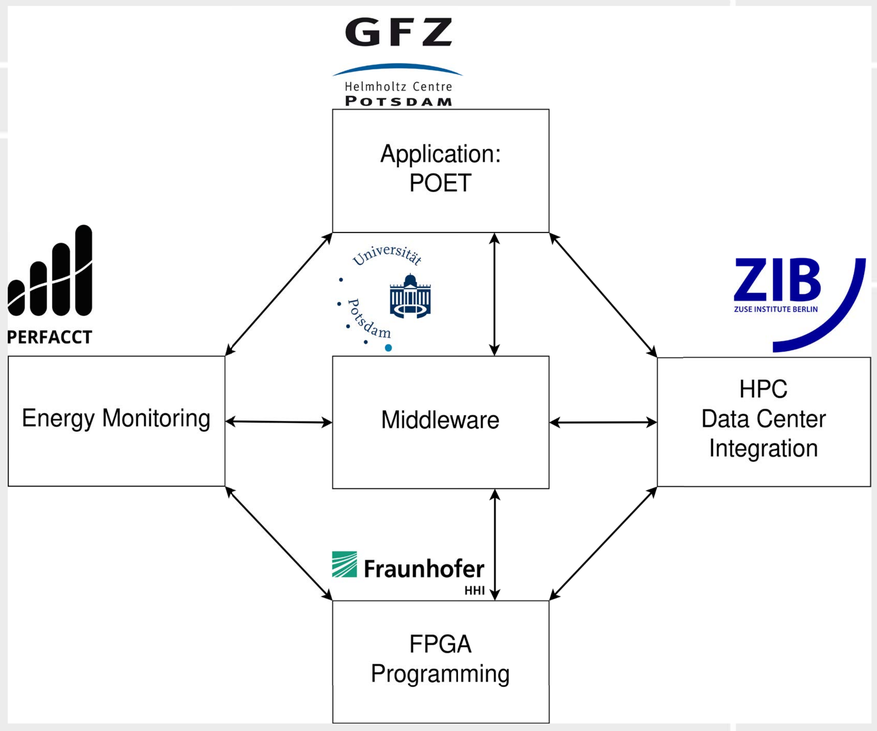
Introduce FPGA-based accelerators as stand-alone network-attached (NA) devices into HPC datacenters:

- Scalable **HW-only**, power efficient accelerator architecture based on State of the Art FPGAs
- Efficient communication via **RoCEv2 / 100Gb Ethernet only** without carrier system
- **HLS-based offloading** of POET (reactive transport simulator) component
- Implementation of a full **RPC Software Stack**

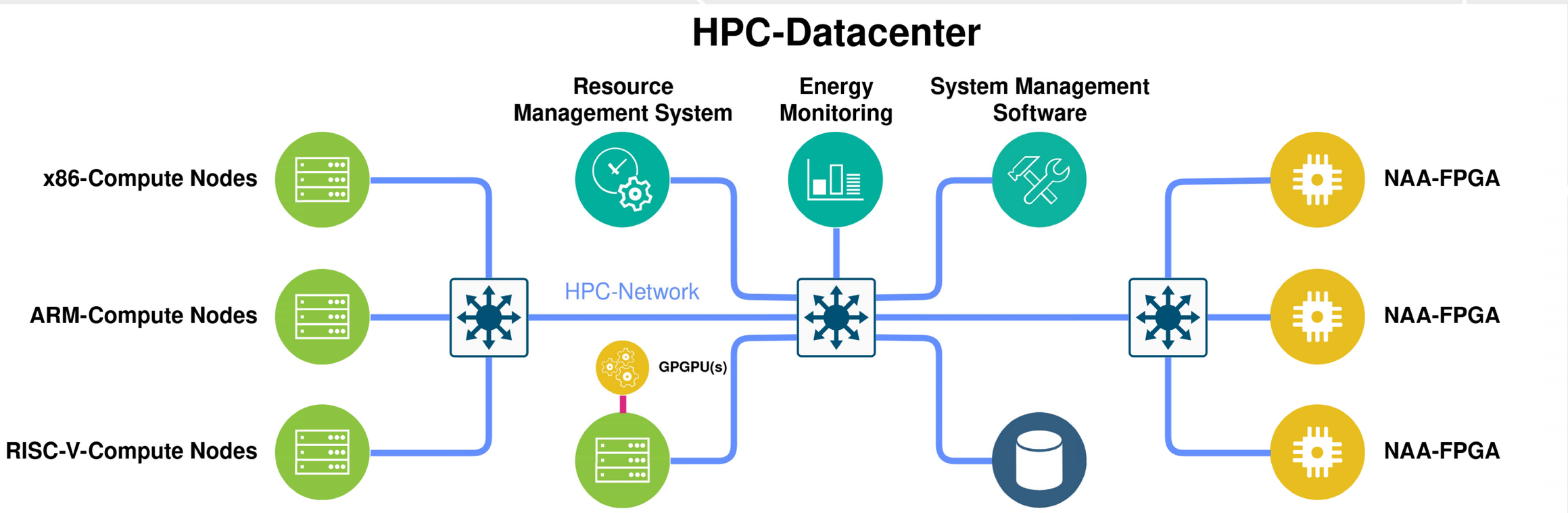
Achieve and monitor higher energy efficiency:

- Novel **Energy Measurement for Applications** (EMA) framework
- NA-FPGAs yield up to 18.8-fold increase in energy efficiency (Steinert and Stabernack (2023) *"FPGA-Based Network-Attached Accelerators – An Environmental Life Cycle Perspective"* doi:10.1007/978-3-031-42785-5_17)

2 Partner Roles



3 Overall Architecture



4 Contact

Prof. Dr. Bettina Schnor,
schnor@cs.uni-potsdam.de
Project Website: greenhpc.eu

5 Project Duration and Funding

- **09/2022 – 09/2025**
- Funded by the Ministry of Education and Research. Grant no.: 16ME0622K

SPONSORED BY THE
Federal Ministry of Education and Research

GEFÖRDERT VOM
Bundesministerium für Bildung und Forschung