

NAAICE

Network-Attached Accelerators in Heterogeneous Computing Environments

Fraunhofer Institute for Telecommunications HHI, GFZ Helmholtz Centre for Geosciences, PERFACCT Performance Acceleration Technologies GmbH, University of Potsdam, Zuse Institute Berlin

NAAICE Project Objectives and Goals

Introduce FPGA-based accelerators as stand-alone networkattached accelerators (NAA) into HPC datacenters:

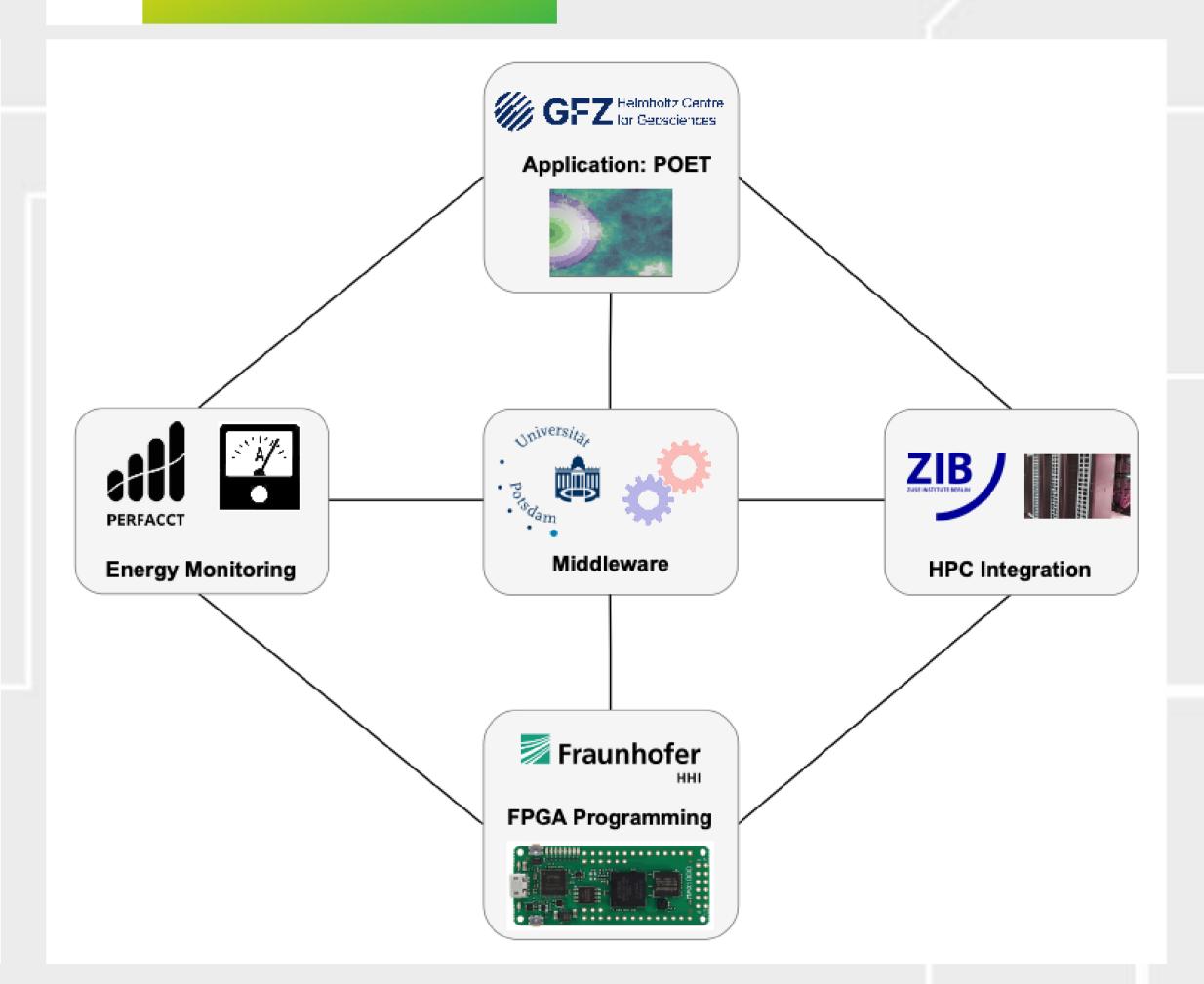
- Scalable, flexible HW-only, power efficient accelerator architecture based on State of the Art FPGAs
- Efficient communication via RoCEv2 / 100Gb Ethernet only without carrier system
- HLS-based offloading of POET (reactive transport simulator) component
- Implementation of a full RPC Software Stack

Integrate different accelerator architectures and monitor energy consumption with novel framework:

"On the Usability and Energy Efficiency of High-Level Synthesis for FPGA-based Network-Attached Accelerators" (2025 doi: 10.1109/IPDPSW66978.2025.00139)



Partner Roles



Overall Architecture

HPC-Datacenter Energy System Management Resource Management System Software Monitoring - ••• - ••• **NAA-FPGA x86-Compute Nodes HPC-Network** 米 · ••• · ••• **ARM-Compute Nodes NAA-FPGA** GPGPU(s) - ••• - ••• - ••• **NAA-FPGA RISC-V-Compute Nodes GPGPU-Nodes** Storage

Contact

Prof. Dr. Bettina Schnor, schnor@cs.uni-potsdam.de Project Website: greenhpc.eu



Project Duration and Funding

- 09/2022 12/2025
- Funded by the Federal Ministry of Research, Technology and Space. Grant no.: 16ME0622K









Gefördert durch:

