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Demonstrator 1: Components for High Performance Computing System Modules (HPC)

Preparing Feasible and Affordable IPs, Interfaces and Workflows plus Accessible Materials and Technologies

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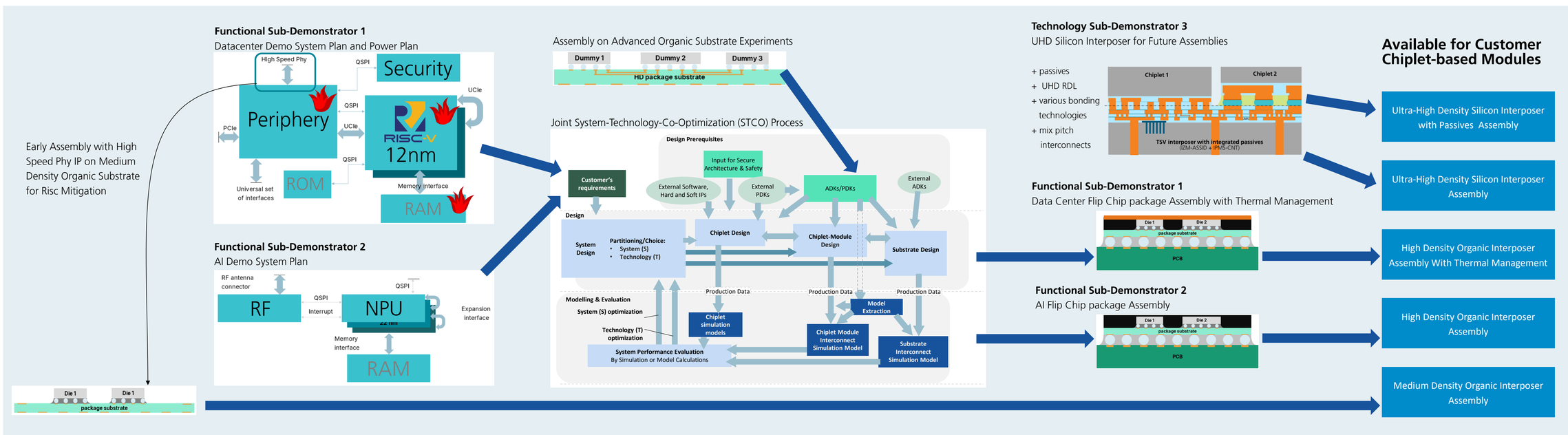

For building a chiplet-based module it seems that there are various possibilities, but when it comes to prototyping the biggest hurdle is to get a prototype manufacturing for small volume. Customer can buy packaging as a service in various volumes, but this does not apply for heterointegration or advanced package, because every implementation is full custom. The HPC Demonstrator will proof a way from system definition to a flip chip package assembly that can be taken for numerous High Performance Computing designs for different applications. These first two demo implementations show feasibility while application to many designs will decrease cost per design and improve access to the technologies even in small volume that will finally be guided by the APECS one stop shop.

STCO for two different HPC systems

The two functional sub demonstrators enter the STCO process with different structure and different objectives. As shown in the table below, the definition of "high performance" differs like the scenarios of operation. Obviously #1 needs a thermal management and #2 does not.

There is also a difference in the interfaces. While the market is demanding UCIe for compute chiplets as used in #1 the UCIe interface will be too complex and power hungry for ultra low power designs like #2. As the highest bandwidth signal defines the effort for substrate RF modelling there are various needs for this as well. Nevertheless, we will show that common technology and methodology complemented by differing efforts and production steps can be used to address different designs.

The STCO of the two different assemblies has to cope with different objectives (examples)

STCO objective	RISC-V compute module #1	AI at the edge compute module #2
Definition of „high performance"	Compute operations per second: TOPS (speed)	Compute operations per watt: TOPS/W (efficiency)
„on" power consumption	? * 10 W	? * 100 mW
"on" to "off" ratio	Always on	Always on and sparsely on
„off" leakage power	mW	10 uW … 100 nW
Highest BW signal	UCIe data lines, 8 GB/s SerDes	2.4 GHz RF

The differences between #1 and #2 are on the design side:

- Standard commercial UCIe and PCIe (#1) vs. custom tailored low power expansion interface and RF link (#2)
- 22 nm FDSOI + 12 nm FinFet full digital design (#1) vs. all 22nm FDSOI RF and Mixed Signal designs (#2)

The flip chip packages will be based on the same technology, but #1 will need additional process steps to add a heat spreader

Outcome for various customer tailored HPC systems

There will be silicon proven IPs for a Security Element, periphery and multi-core-RISC-V computing as well as an ultra low power 2.4 GHz wakeup RXTX that can also be used as a RF band scanner and a Mixed-Signal DNN Neuromorphic Processing Unit. There will be also at least one RISC-V core in the Security, Periphery and NPU chiplets. A combination of any number of any of the chiplets can be used in a customer design to address various use cases. This is ensured by a common (Q)-SPI interface infrastructure for basic interoperability.

The most commonly demanded UCIe and LP-DDR4 interfaces as well as some more memory interfaces will be available as silicon proven interface IPs and therefore with a reasonable price and time to market. HBM is already available from another project.

There will be ADKs/PDKs for at least two featured substrate technologies and a lot of workflow experience.

Assembly on advanced organic substrate with 120 µm pitch related to UCIe Standard
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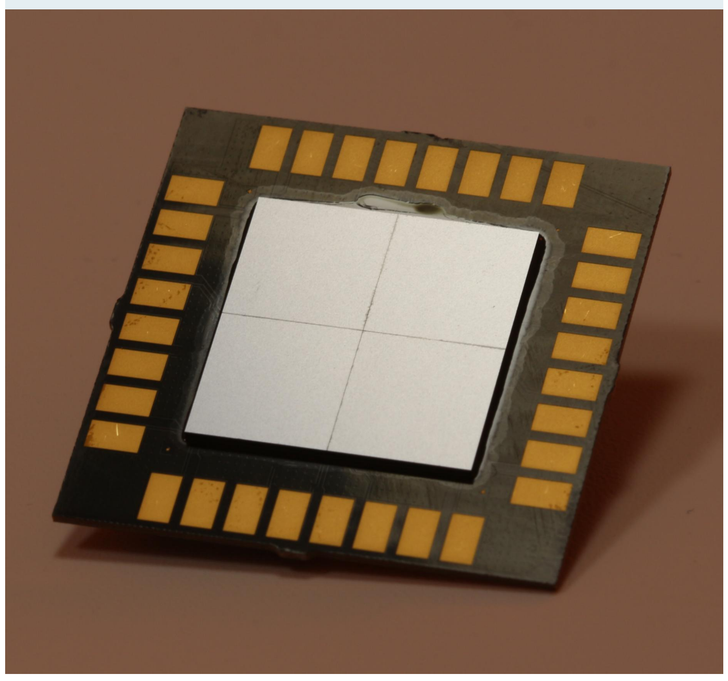

Technology Sub-Demonstrator 3 addresses building blocks for future HPC systems. Increasing IO density and the need for integration of chiplets from very much different technologies demand for new options:

- Ultra-high density RDL and fine pitch interconnect formation
- Enable different methods of bonding on the same interposer
- Add passive functions in the silicon interposer
- Mix-pitch interconnect technologies

Examples for these technologies are shown in the technology sub-demonstrator #3 to prepare technologies to be ready for future assemblies.

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Additional information

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