

Contributions to the APECS Pilot Line: Fraunhofer ENAS

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Fraunhofer ENAS is one of 14 German research institutes involved in the implementation of the APECS pilot line. It supports customer projects from the initial idea and design phase, through technology development or implementation using existing technologies, all the way to a fully tested prototype.

The role of Fraunhofer ENAS in the APECS pilot line

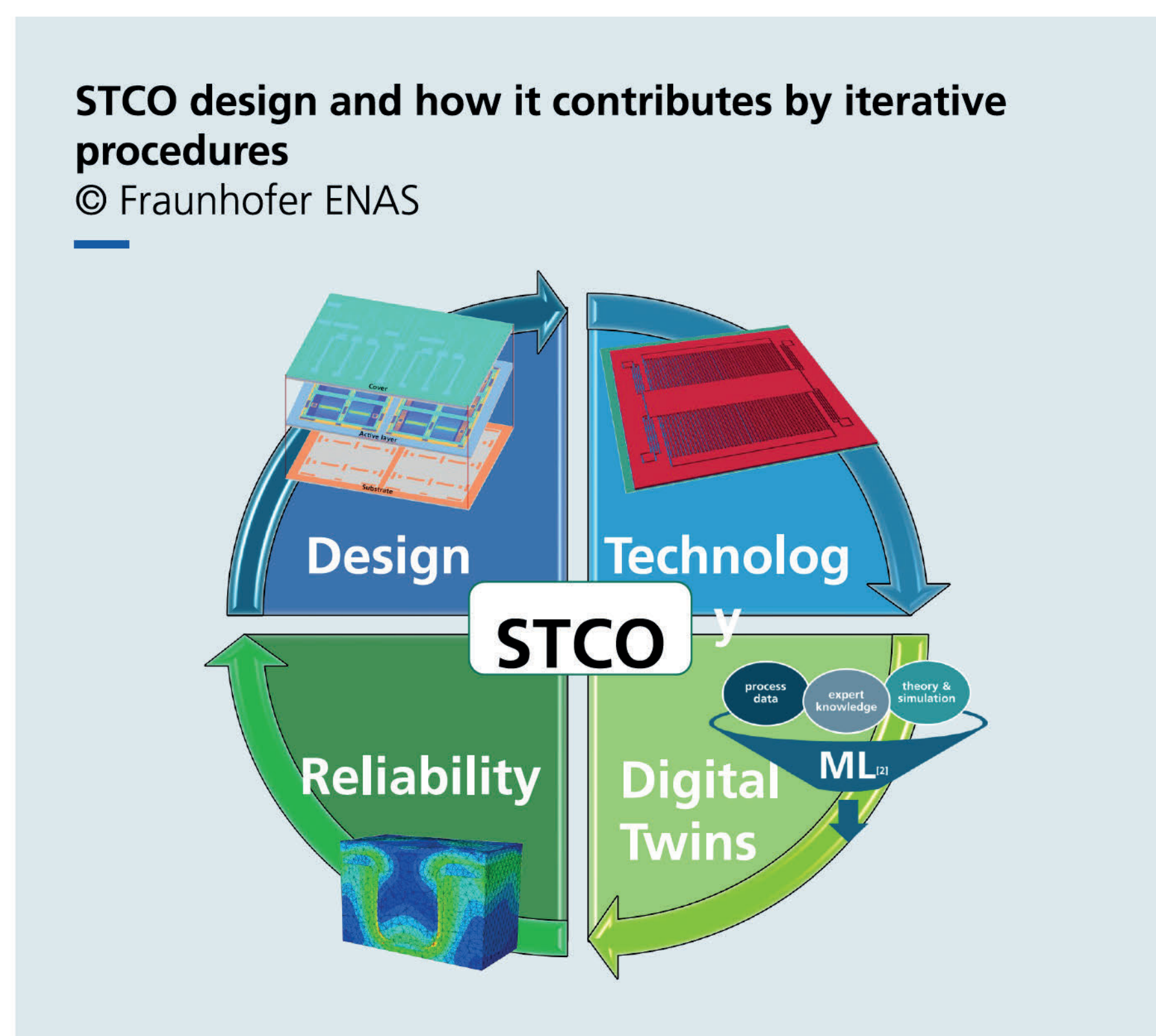
Fraunhofer ENAS collaborates with the other institutes of the Research Fab Microelectronics Germany (FMD) on a pilot line for the development and manufacture of highly integrated electronic systems. Applications range from high-performance computing and high-speed data transfer to quantum computing. It is contributing expertise in wafer and chip integration, interposer and chiplet technologies including flexible interposers, as well as the production of compatible contacting materials and linking them with new fields such as neuromorphic computing and quantum technologies.

Contributions to the APECS pilot line

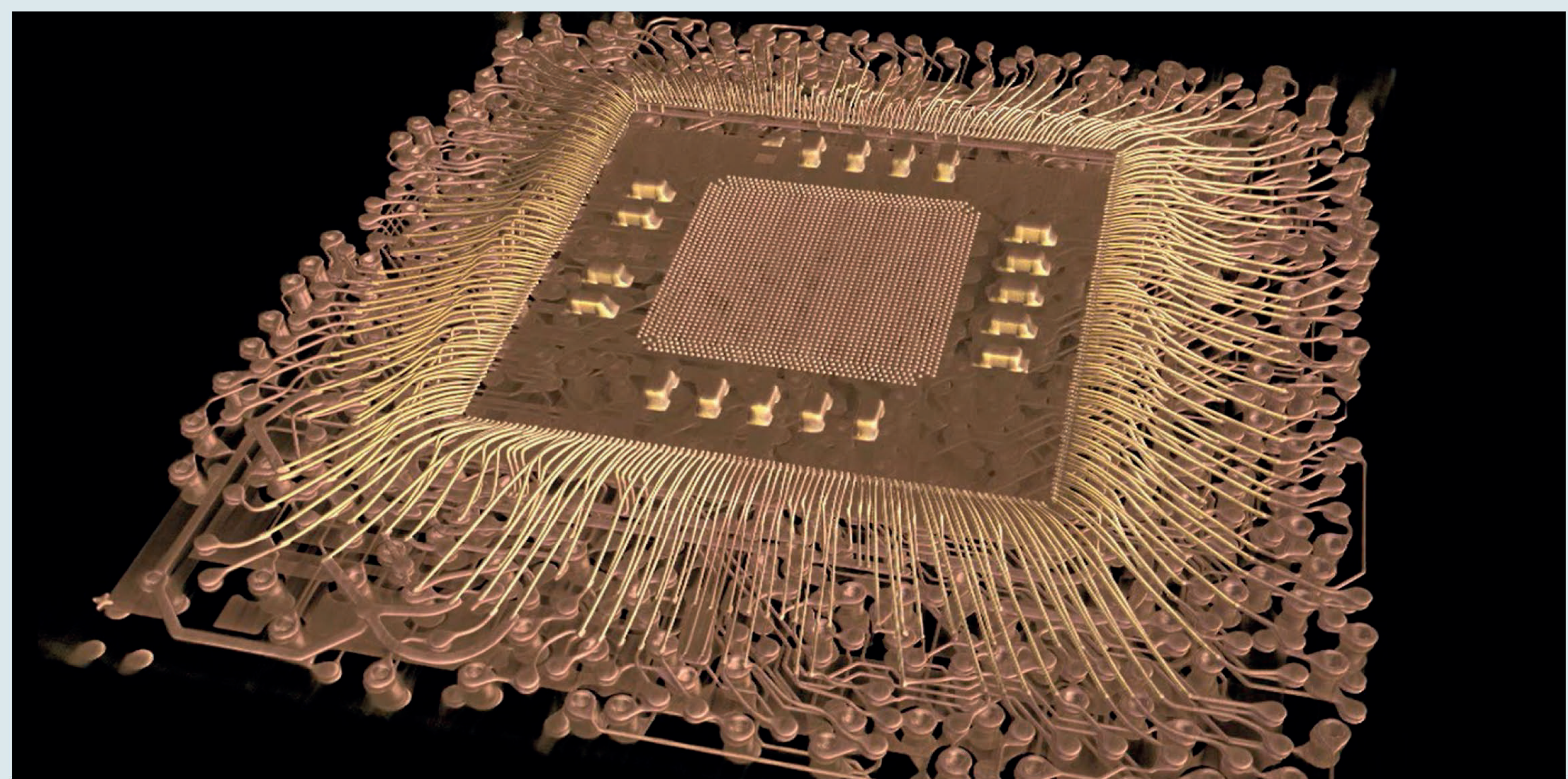
STCO design enablement:

Fraunhofer ENAS provides designs and design workflows for 2.5D/3D heterogeneous integration, contributes to PDKs/ADKs, as well as to modeling for the numerical optimization of manufacturing processes. Specific workflows and the necessary mutual coordination and adaptation of the design including all necessary details (e.g. interface pads, material compositions, function, design for test and for fabrication, mask generation) are developed. The target is a modular, technology-independently flexible design flow with interfaces to the fabrication and to the test automation. Process designs and surrogate models for advanced and novel processes towards multi-technology integration is done for deep ion etching of Si (feature scale model) for MEMS, beyond CMOS and 3DHI applications, chemical mechanical planarization (chip and feature scale models) for 3DHI applications and wafer bonding (wafer scale model) for 3DHI applications.

Model based optimization of multi-technology flows using physics-based process models running on high-performance computing hardware and the establishment of surrogate models of semiconductor processes as digital twins for virtual prototyping, advanced process control and virtual metrology as prototype solutions for the FMD are implemented during the implementation phase. Self-contained digital models for individual process steps require novel interfaces to establish process chain models along semiconductor processing workflows as technology models.



Visualization of a micro chip module on top of a printed circuit board by x-ray computer tomography. Investigations of details and sectional views with high resolution become possible.
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Test and reliability analysis:

Fraunhofer ENAS works on developing a broad spectrum of characterization, testing, and reliability methods, including 2.5D/3D and optical tests, electrostatic sensitive device (ESD) and electromagnetic compatibility (EMC) reliability testing, as well as analyzing thermomechanical reliability aspects – complemented by modeling and numerical reliability evaluations. Burn-in testing at the module and wafer levels, as well as the associated AI-based data analysis is being developed to provide efficient methods for assessing reliability and providing corresponding feedback to manufacturing processes.

Packaging technologies:

Chip-to-wafer and wafer-to-wafer bonding processes are a key focus area that has reached a high level of sophistication through continuous development at Fraunhofer ENAS in recent years. As a result, various bonding processes based on inorganic insulating and metallic interlayers, as well as polymer interlayers, and processes for so-called direct bonding without interlayers are available for use and are being qualified for the pilot line in a way that enables the efficient production of pilot batches. One of the most productive processes is hybrid bonding. Electronic circuits are vertically interconnected at the wafer level, whereby an insulating interlayer is interrupted at specific locations and replaced by metallic signal-carrying connections. TSV fabrication, high-aspect-ratio etching, electroplating (Process IntraCu® SC-4), and CMP processes are used to prepare the compatible wafers before they are bonded together through direct bonding.

Cross section of the interconnection of two wafers as a result of hybrid bonding. Copper plugs (brighter areas in the image) are the electric connections between an upper and a lower wafer and are arranged within recesses of isolation layers (darker areas).
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What is APECS?

APECS (Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems) is one of 5 European pilot lines established under the EU Chips Act. APECS is the foundation for Europe's competitive position in heterogeneous system integration and advanced packaging. It plays a vital role in enhancing Europe's strategic autonomy by reducing dependence on foreign suppliers and strengthening Europe's capabilities in critical technology areas.

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Additional information

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