

Contributions to the APECS Pilot Line: Fraunhofer IIS

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Fraunhofer IIS is one of 14 German research institutes involved in the implementation of the APECS pilot line. As one of the 12 Fraunhofer institutes, Fraunhofer IIS brings in-depth expertise in the design, integration, characterization, and testing of chiplets. This includes advanced IP development and system-level integration, which are key to enabling scalable chiplet-based architectures.

The role of Fraunhofer IIS in the APECS pilot line

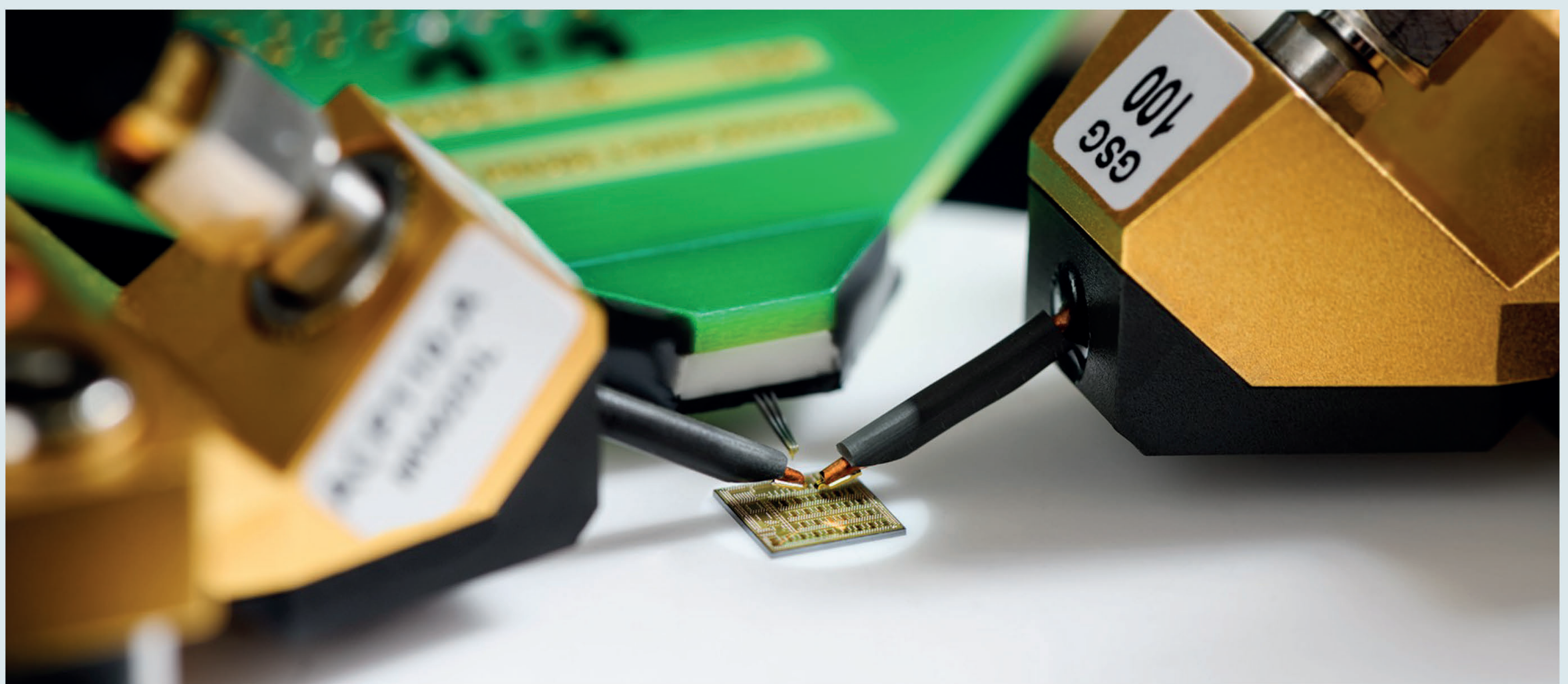
Next to its leading role in STCO design, it also has the lead for the development of a high-performance computing (HPC) demonstrator to validate the capabilities of the pilot line. The work at Fraunhofer IIS is carried out across 3 divisions:

- Smart Sensing and Electronics: combining sensing, electronics, and system integration, as well as assessing the reliability and performance of modern chiplet-based solutions.
- Engineering of Adaptive Systems: developing methods and technologies for chiplet-based architectures, particularly for adaptive and high-performance electronic systems. A key focus is on a holistic approach to design, integration, and testing.
- Development Center X-ray Technology: proven expertise in high-resolution X-ray-based analysis and characterization of electronic assemblies. These methods are essential for quality assurance, failure analysis, and the reliability assessment of modern packaging and integration technologies.

The close integration of design, integration, analysis, and validation enables the development of robust, industry-ready solutions for future microelectronic systems.

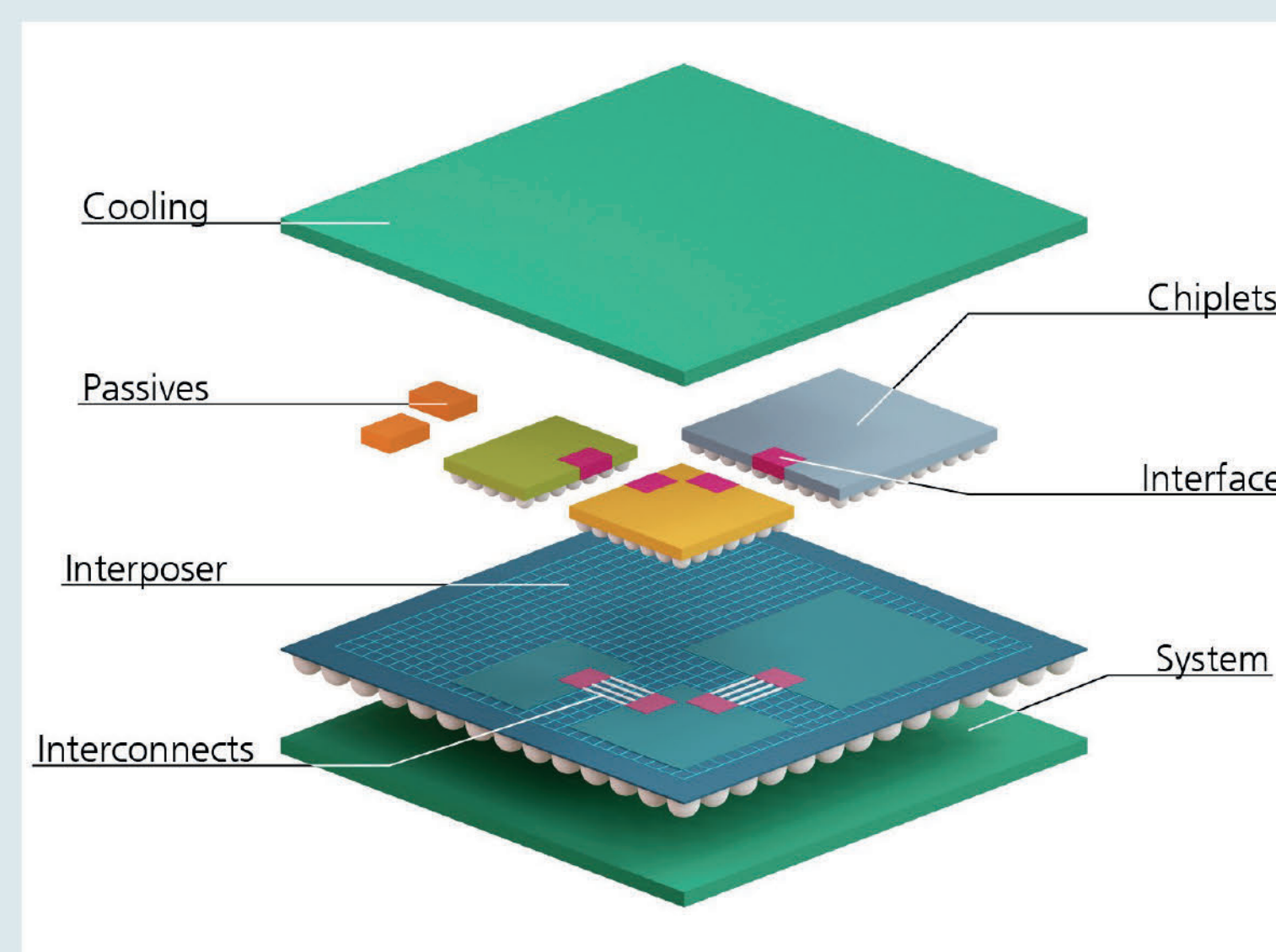
Reliability testing

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Electronics solutions based on chiplets are the first to allow the integration of various functional units in different technologies on a substrate or into a 3D chip structure

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What is APECS?

APECS (Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems) is one of 5 European pilot lines established under the EU Chips Act. APECS is the foundation for Europe's competitive position in heterogeneous system integration and advanced packaging. It plays a vital role in enhancing Europe's strategic autonomy by reducing dependence on foreign suppliers and strengthening Europe's capabilities in critical technology areas.

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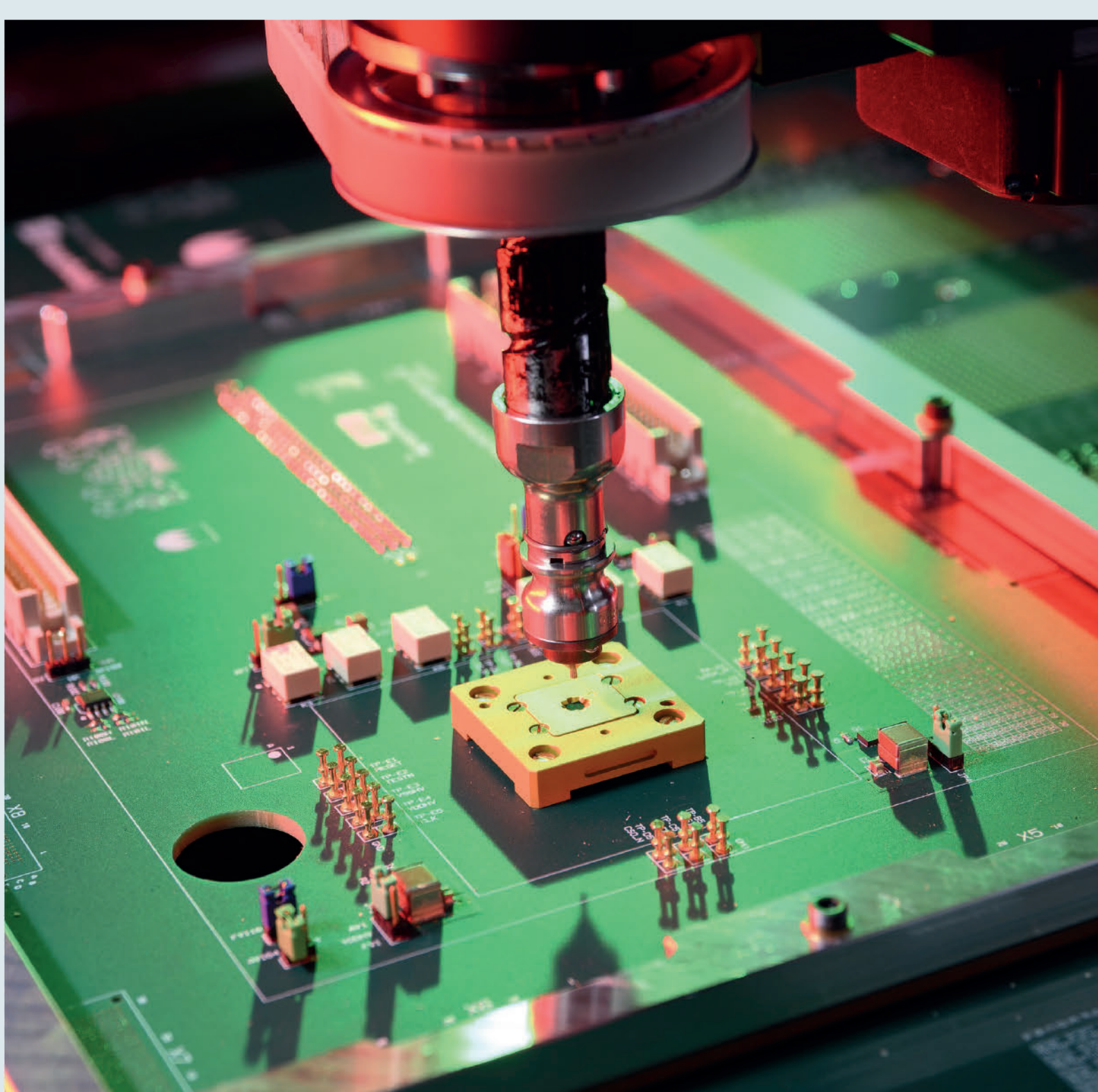
Additional information

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Views and opinions expressed are however those of the author(s) only and do not necessarily reflect those of the European Union or the Chips Joint Undertaking. Neither the European Union nor the granting authority can be held responsible for them.

Test engineering and small-series testing of various chips

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Technological focus areas

As part of APECS, Fraunhofer IIS contributes extensive expertise across the entire microelectronics value chain. Our activities span chip and system design, system-level integration, and the characterization, testing, and failure analysis of modern chiplet-based systems.

- Implementing an STCO Design methodology for the APECS pilot line including IP enablement for chiplets, chiplets for X, ADK & PDK development for 2.5D/3D and QML, and design tools for system modeling
- Providing a portfolio of chiplets having means for RISC-V and mixed-signal AI computing, from low power to high-speed interfacing, analog, sensor and RF signal processing and for security features
- Expanding equipment and methods for the characterization and testing of chiplets and heterogeneous systems, including non-destructive X-ray-based defect detection.