

Contributions to the APECS Pilot Line: Fraunhofer IZM-ASSID

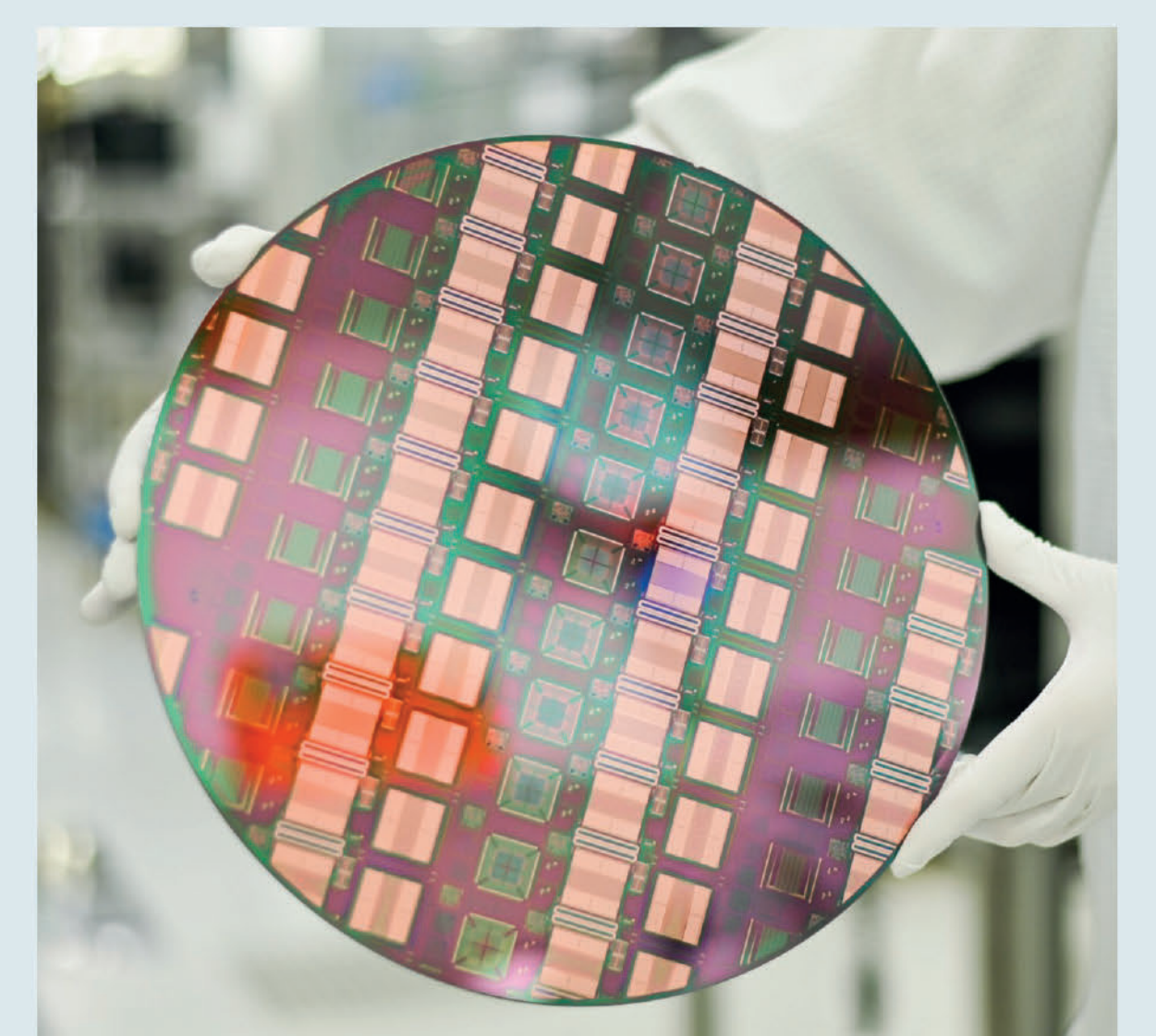
Authors: Frank Windrich, Kathrin Reinhardt, Steffen Bickel, Kay Viehweger, Manuela Junghänel

Fraunhofer IZM-ASSID contributes advanced wafer-level packaging and heterogeneous integration technologies to the APECS Pilot Line, strengthening Europe's capabilities in next-generation semiconductor systems. Operating a 200 mm and 300 mm industry-compatible cleanroom infrastructure, IZM-ASSID provides key technologies for chiplet-based system integration, including silicon and glass interposers, redistribution layers, TSV integration, wafer bonding, hybrid bonding, and ultra-fine-pitch interconnects.

Within APECS, Fraunhofer IZM-ASSID enables the realization of high-performance, energy-efficient electronic systems through advanced 2.5D and 3D integration approaches. As a technology provider for the European chiplet ecosystem, ASSID supports the development, prototyping, qualification, and transfer of advanced packaging solutions from research to industrial deployment.

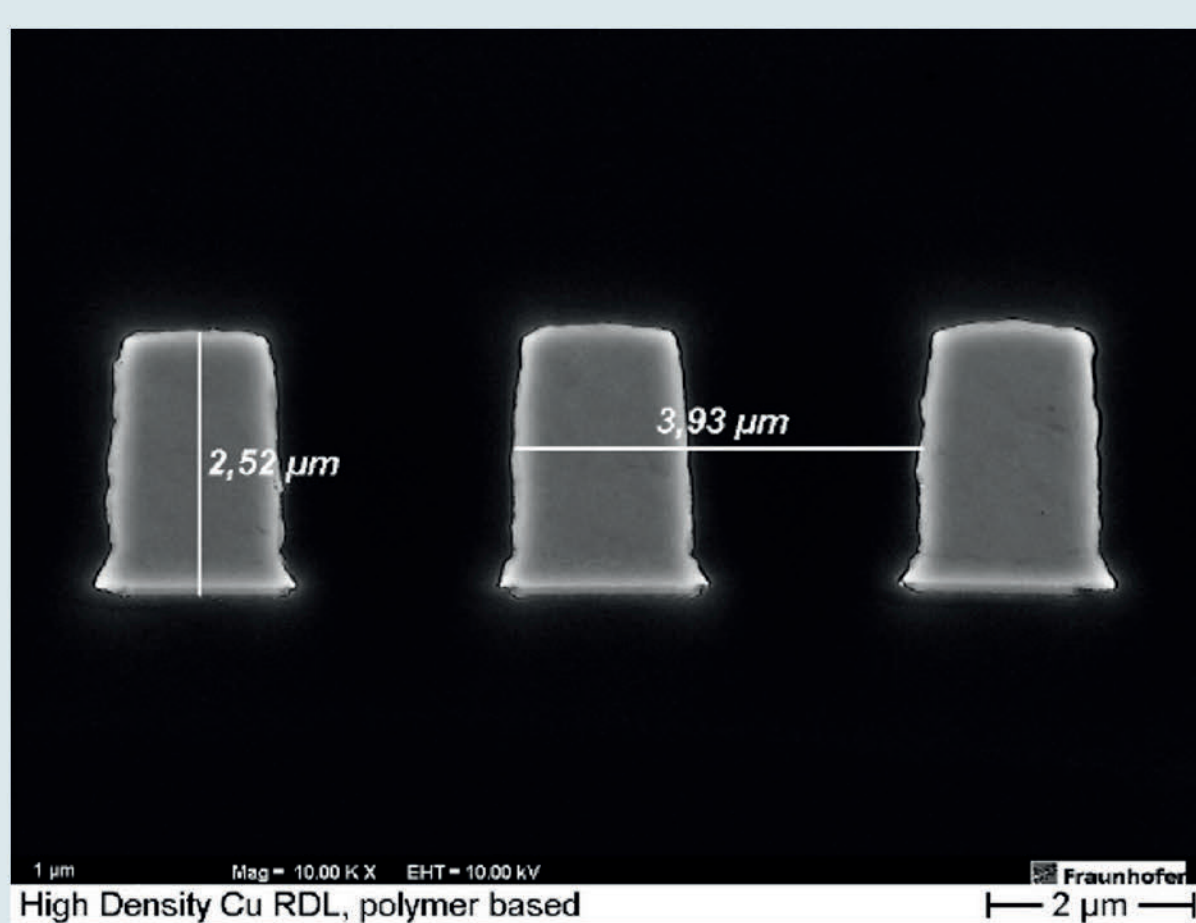
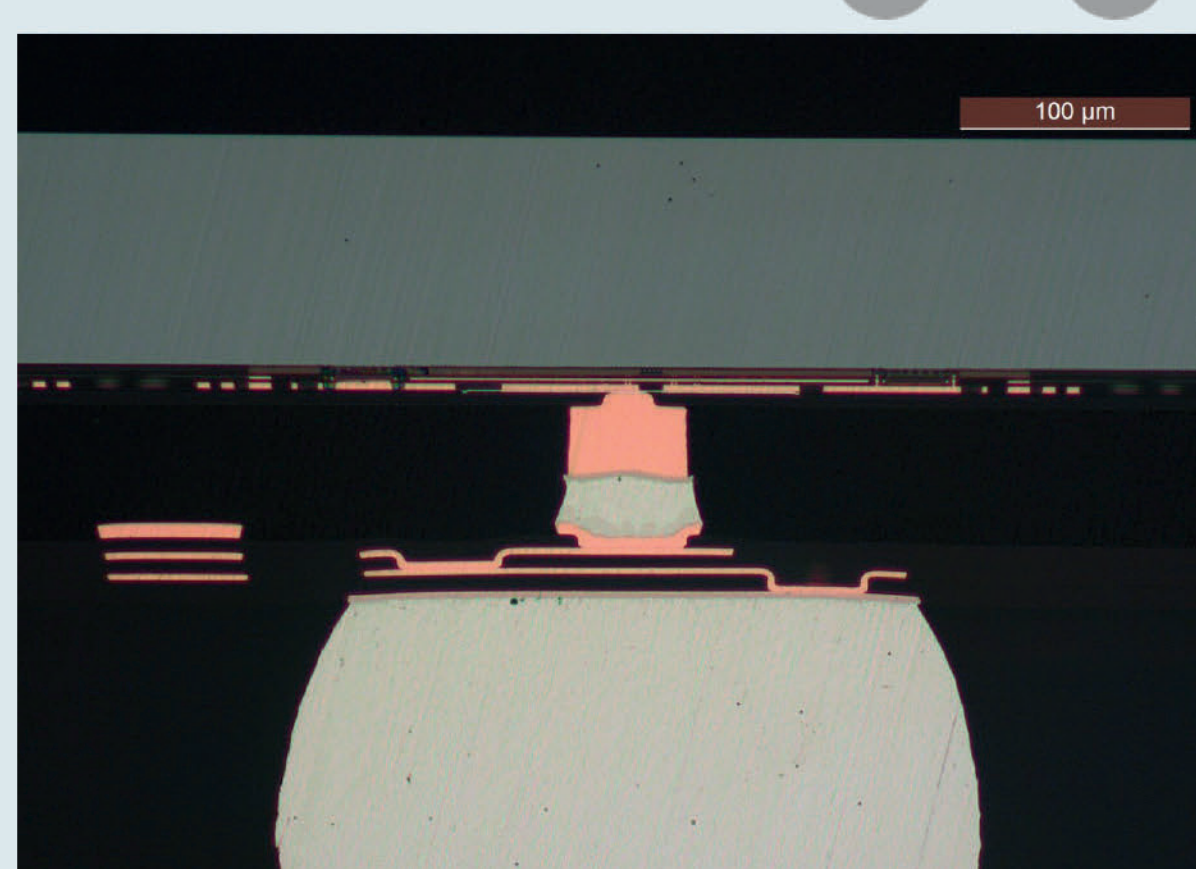
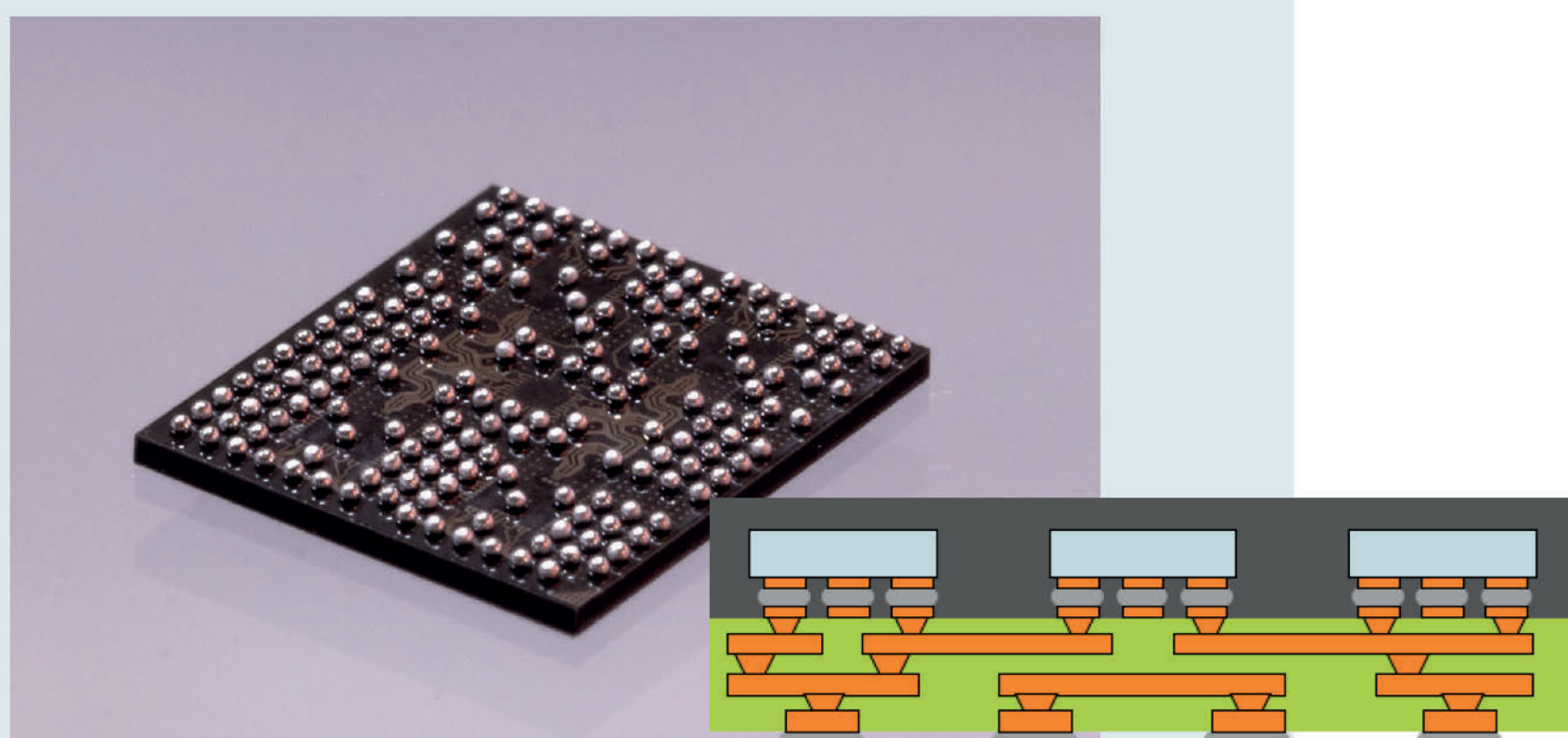
300 mm Wafer-level packaging pilot line at Fraunhofer IZM-ASSID (L), 300 mm Si interposer wafer with microfluidic cooling function (R).

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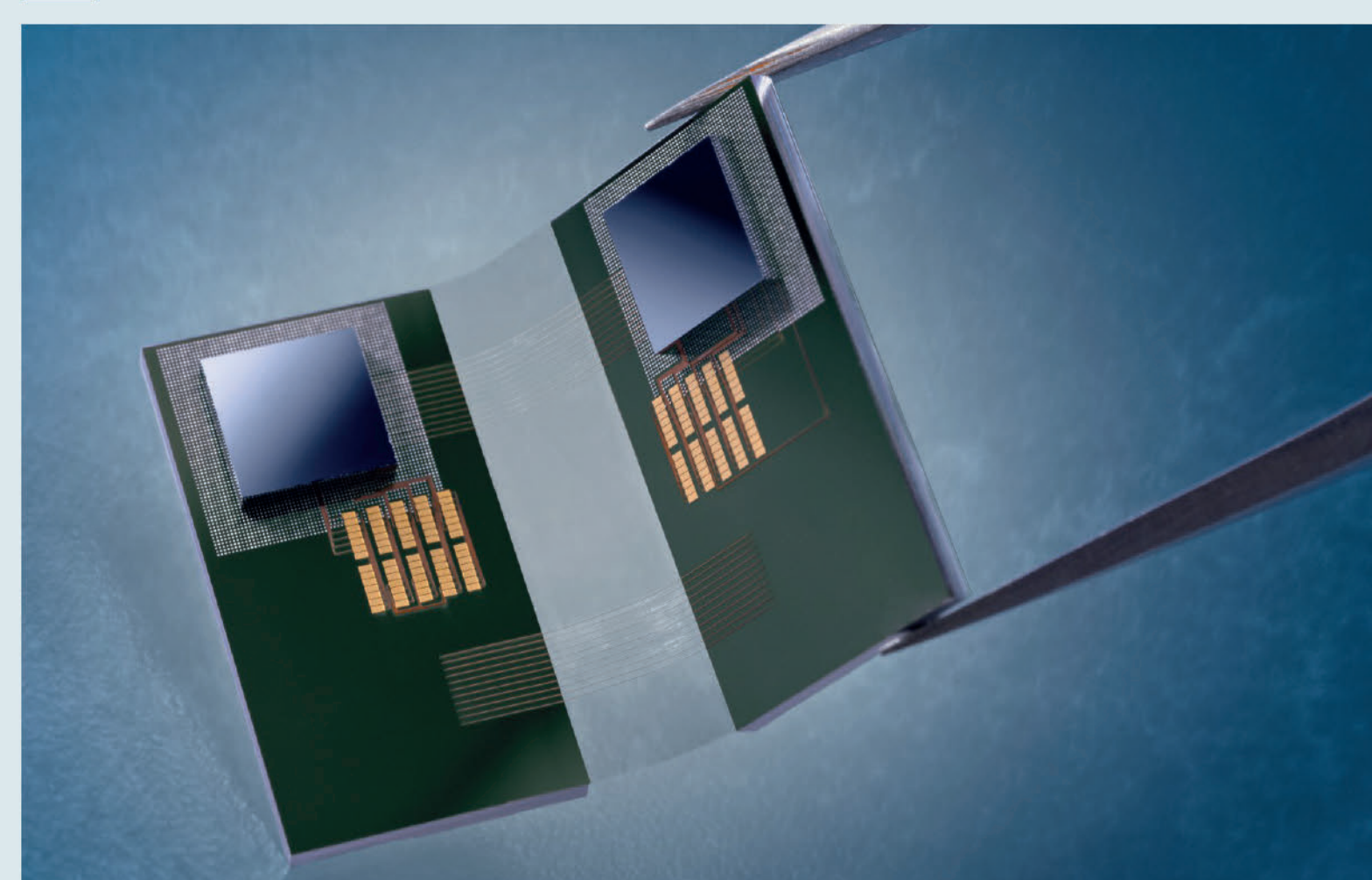
Customized System in Package (SiP) using RDL1st Fan Out Wafer-Level Packaging.

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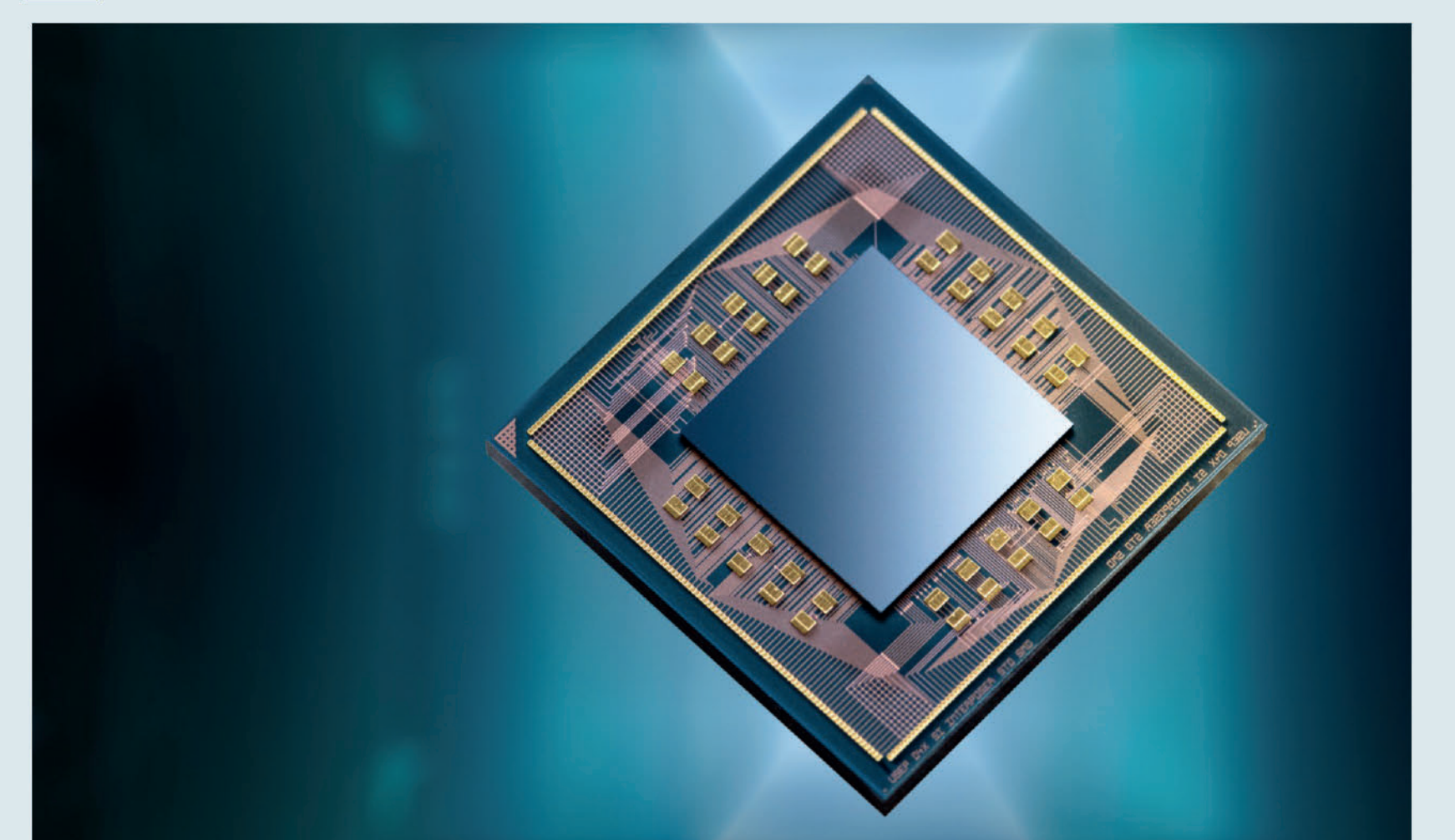
System in Package: Rigid-flex Si interposer chiplet system for cryo applications.

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Processor die assembled on high density Si interposer – D2W integration.

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Fraunhofer IZM-ASSID in APECS: Role, Capabilities & Technology Building Blocks

200/300 mm industry-compatible wafer-level packaging process line // ISO 9001 certified management system

Customized System in Package SiP solutions:

- Cu-TSV integration: via-middle & via-last, TSV reveal & backside processing
- RDL1st Fan Out Wafer-Level Packaging
- Rigid-flex Si-interposer systems
- Microfluidic Si-Interposer with integrated cooling

Ultra-high density interposer substrates:

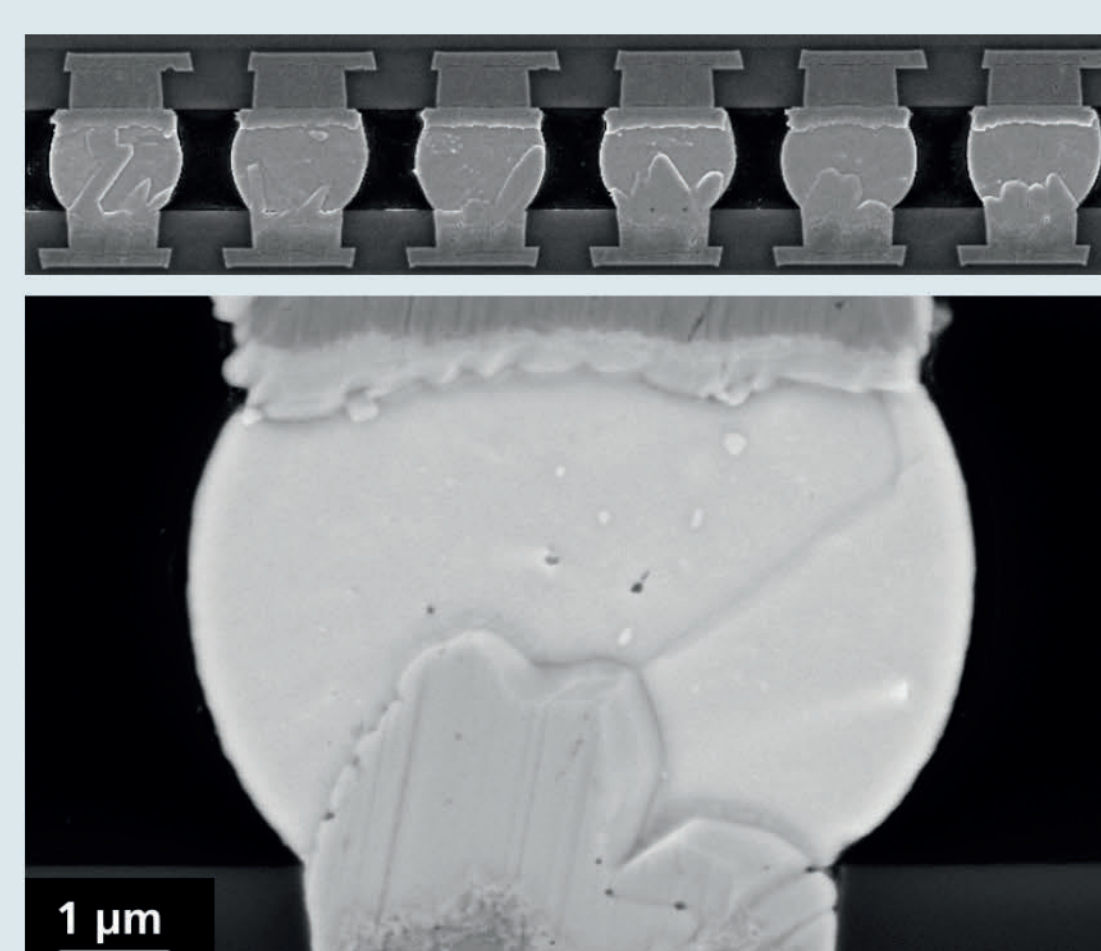
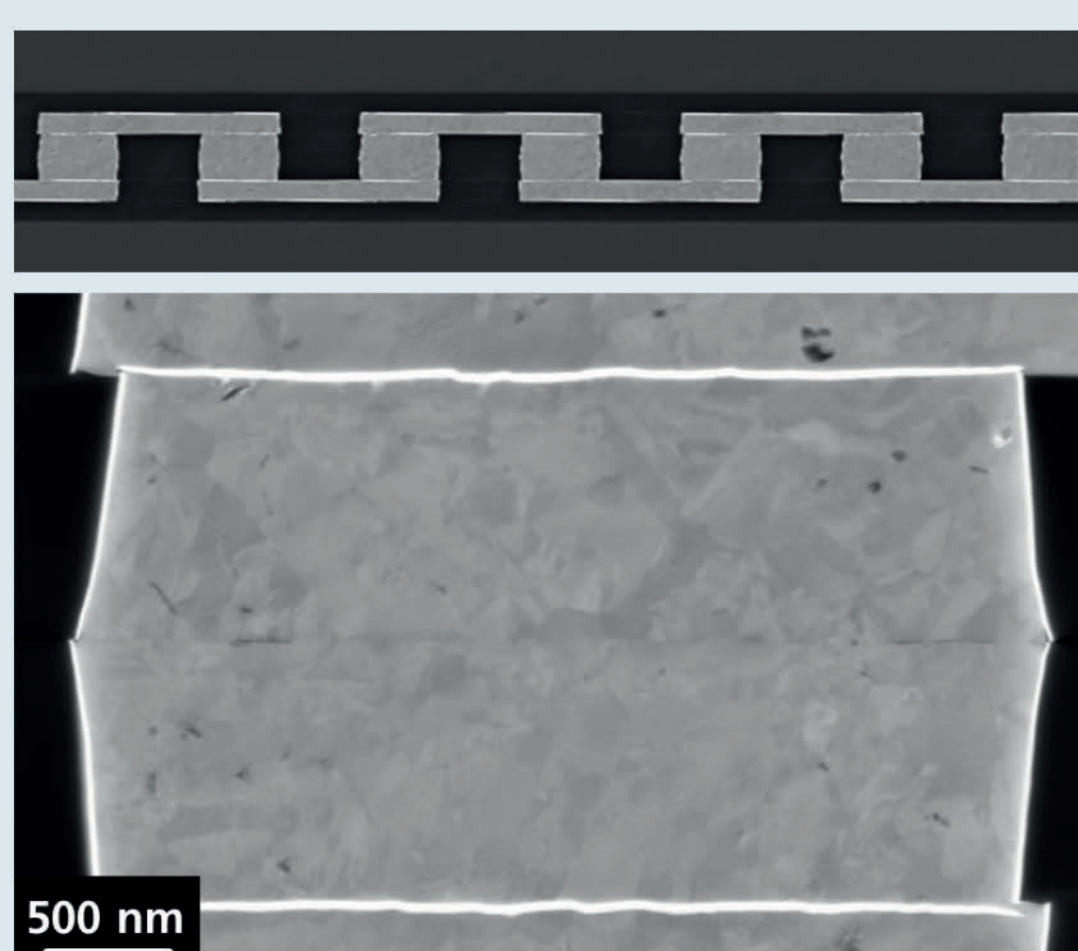
- Si and glass interposers with TSV/TGV and multilayer redistribution
- Si-bridge fabrication with integrated passives
- High-density frontside/backside interconnects and wafer-level bumping
- Fine pitch assembly: hybrid bonding, TCB, mass reflow
- Superconducting RDL ($T_c > 4$ K)

3D heterogeneous quasi-monolithic integration and stacking:

- Die to wafer (D2W), Die to die (D2D) & Wafer to wafer (W2W) integration
- Wafer-scale integration for high performance computing

Integration technologies: Cu/SiO₂-hybrid-bond (L) and Cu/Ni/SnAg microbump interconnects (C) and Cu-TSVs (R).

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Additional information

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Views and opinions expressed are however those of the author(s) only and do not necessarily reflect those of the European Union or the Chips Joint Undertaking. Neither the European Union nor the granting authority can be held responsible for them.