

Contributions to the APECS Pilot Line: Fraunhofer IZM

Authors: Braun, Tanja; Schiffer, Michael

Fraunhofer IZM is one of 14 German research institutes involved in the implementation of the APECS pilot line.

2.5D & 3D Chiplet integration platform

Fraunhofer IZM serves as technology hub for all aspects of chip and chiplet integration. The necessary elements to provide access to the value chain from chip(let) to functional system encompass:

- Si interposers, offering TSVs and re-routing for highest interconnect densities
- Non-Si interposers for special applications like optical integration, MEMS/Sensor/LWG integration as well as large format organic interposers
- Chiplets and chip preparation for 2.5D integration onto interposers, offering sub 10 μm interconnect densities
- W2W & D2W stacking for shortest interconnect paths (both with microbumps and hybrid bonding)
- High-speed assembly of chip(let) modules onto HD PCB
- Fan-out system scale integration for chips and chiplets
- System integration from chip(let) down to system board including stiffener, heatsink, power supply etc.

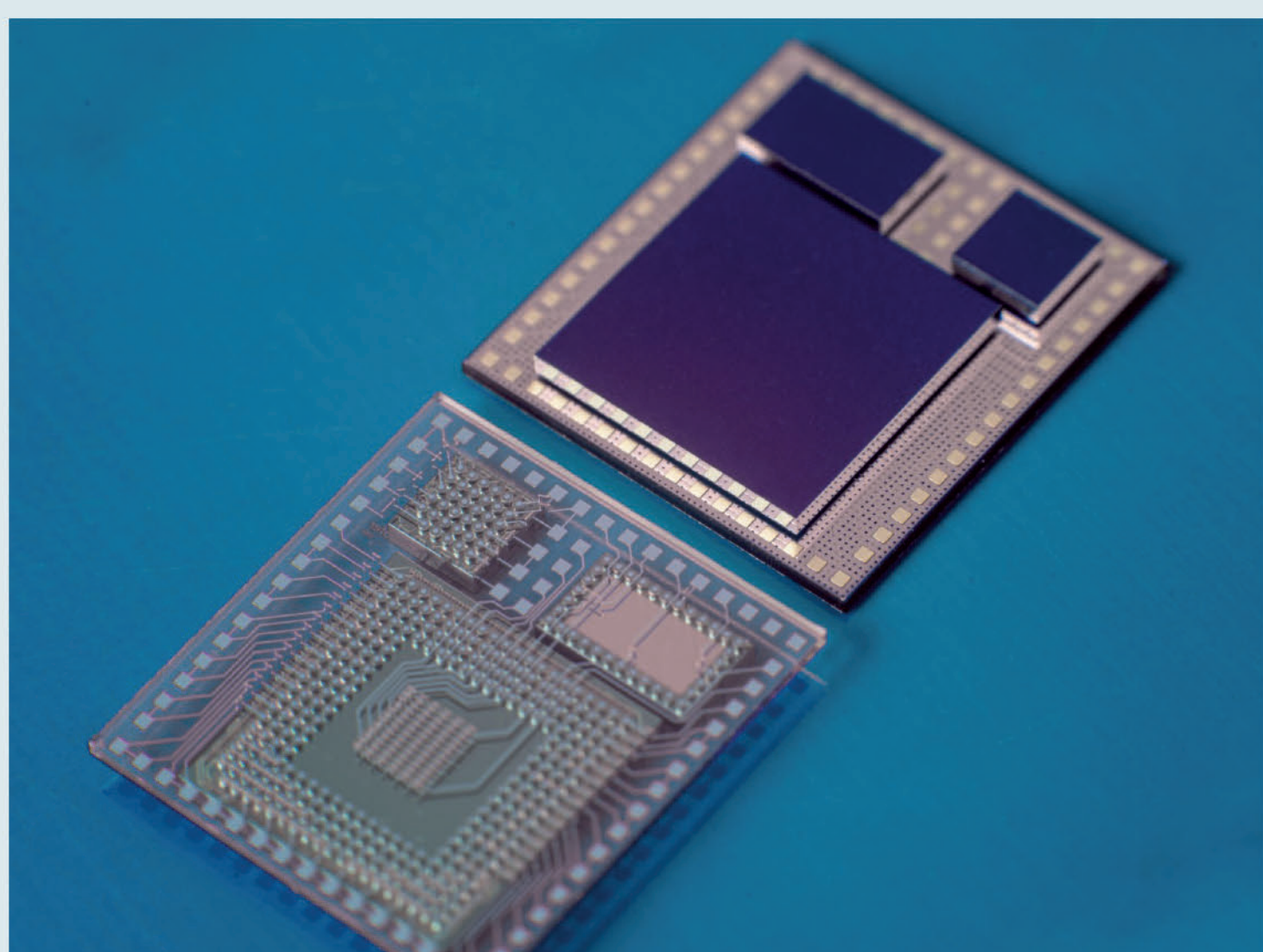
All provided technologies are implemented on industry scale infrastructure for easy transferability and service offers.

Service offer

- State-of-the-art integration of system partitions (chiplet, ASIC, sensors) in and on wafer scale or organic interposers and embedded in PCB or FO-PLP/WLP
- Stack integration of chip/let using microbumps and hybrid bonding (both inorganic and with IM layer)
- Interposers with HD-RDL and microTSVs on Si wafers with supplemental functionalities (R-C-L), resp. Glass for E/O applications
- High speed microcomponents ($\sim 10 \mu\text{m}$ size) placement by μTP
- HD organic interposer and PCBs as well as glass core substrates
- Heterogeneous system integration incl. e.g., high-speed interconnection or antenna attach
- Package and system encapsulation for reliable application
- Design, simulation and validation of electrical, thermo-mechanical or mechanical aspects
- Reliability testing and failure analytics

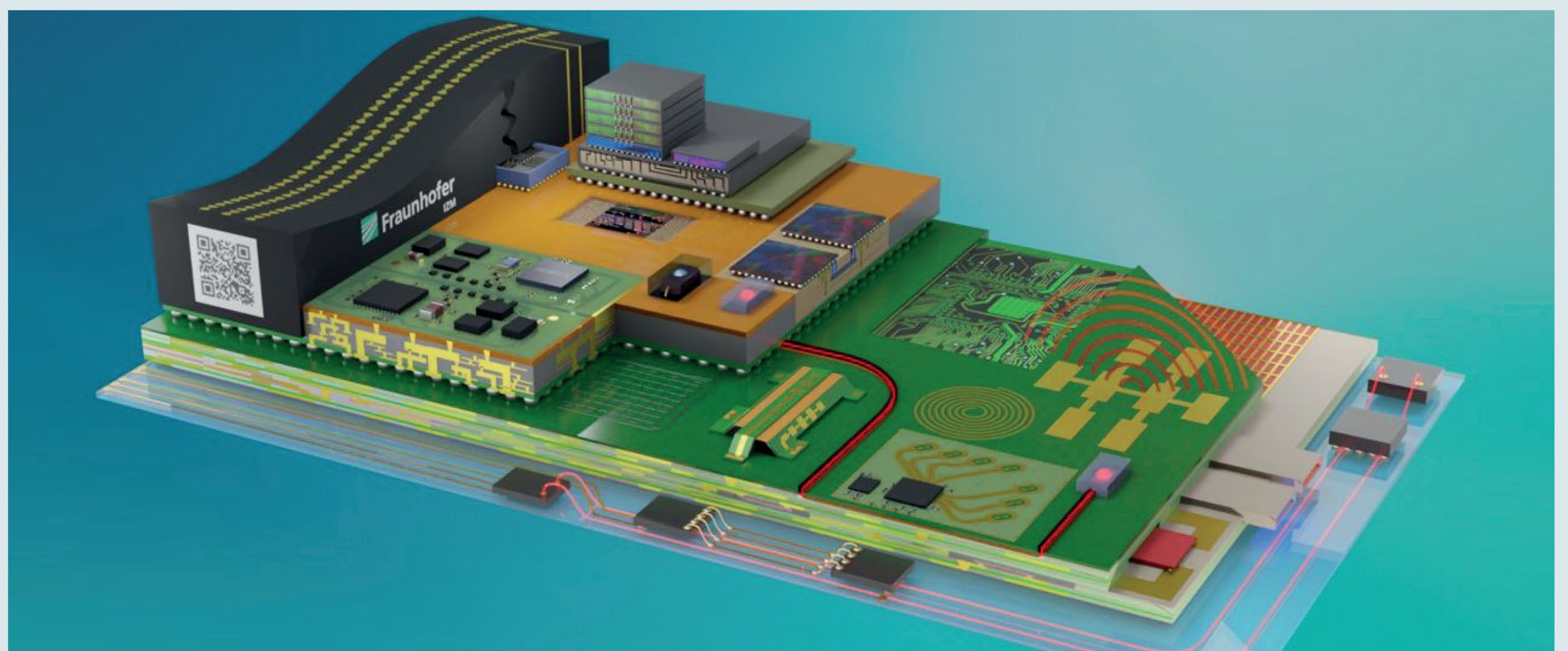
Glass interposer with TGVs and multi-layer RDL with assembled test chiplets

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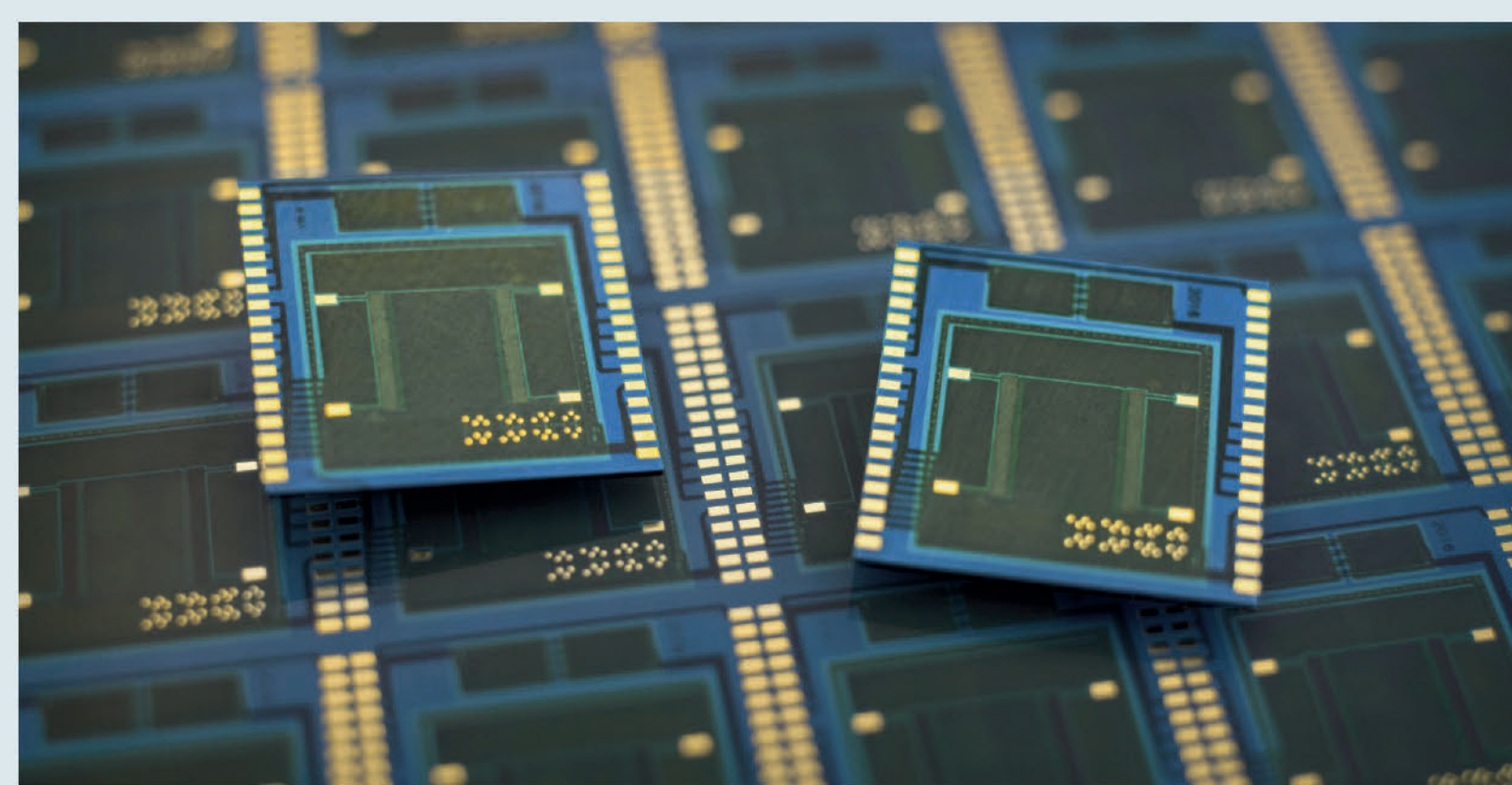
High-end performance packaging from wafer to system

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Fan-out system scale integration on panel level

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Contributions to the APECS pilot line

A key focus within APECS is the development and supply of technological process chains for component and chiplet integration. Using advanced packaging technologies this pilot line aims to implement a chiplet-based system concept. Fraunhofer IZM supports this goal through its technical expertise and application-driven research, helping to improve the long-term resilience of Europe's microelectronics sector.

- Developing innovative assembly techniques for high-density interposers and PCBs, including silicon-based interposers with contact pitches shrinking from 15 μm to below 1 μm
- Pursuing multiple integration approaches (2D, 2.5D, 3D), with an emphasis on thermal management and minimizing hotspots
- Providing comprehensive test environments to verify the functionality of individual chiplets after their integration
- Design substrates that support ultra-fine structures down to 1 μm , using novel materials such as glass, particularly relevant for AI and high-performance computing
- Enabling more modular, reusable, and cost-efficient chiplet systems by integrating multiple specialized chiplets onto a single substrate

What is APECS?

APECS (Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems) is one of 5 European pilot lines established under the EU Chips Act. APECS is the foundation for Europe's competitive position in heterogeneous system integration and advanced packaging. It plays a vital role in enhancing Europe's strategic autonomy by reducing dependence on foreign suppliers and strengthening Europe's capabilities in critical technology areas.

Contact

Dr. Tanja Braun

Head of System Integration & Interconnection Technologies

Phone: +49 30 46403-244

Email: tanja.braun@izm.fraunhofer.de

Dr. Michael Schiffer

Head of Wafer Level System Integration

Phone: +49 30 46403-234

Email: michael.schiffer@izm.fraunhofer.de

Fraunhofer Institute for Reliability and Microintegration IZM
Gustav-Meyer-Allee 25, 13355 Berlin, Germany

www.apecs.eu | info@apecs.eu

Additional information

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