

Contributions to the APECS Pilot Line: Leibniz IHP

Authors: Wietstruck, Matthias; Panic, Goran; Mai, Andreas;

Leibniz IHP is one of 14 German research institutes cooperating to establish the APECS pilot line. As one of the two participating Leibniz institutes, it conducts R&D across a broad range of fields, including RF and broadband systems, resilient systems, sensory systems, intelligent edge technologies, advanced semiconductors, and device and material innovation.

Its research focuses on economically relevant topics with applications in telecommunications, the semiconductor industry, aviation, automation technology, telemedicine, and other sectors.

The role of Leibniz IHP in the APECS pilot line

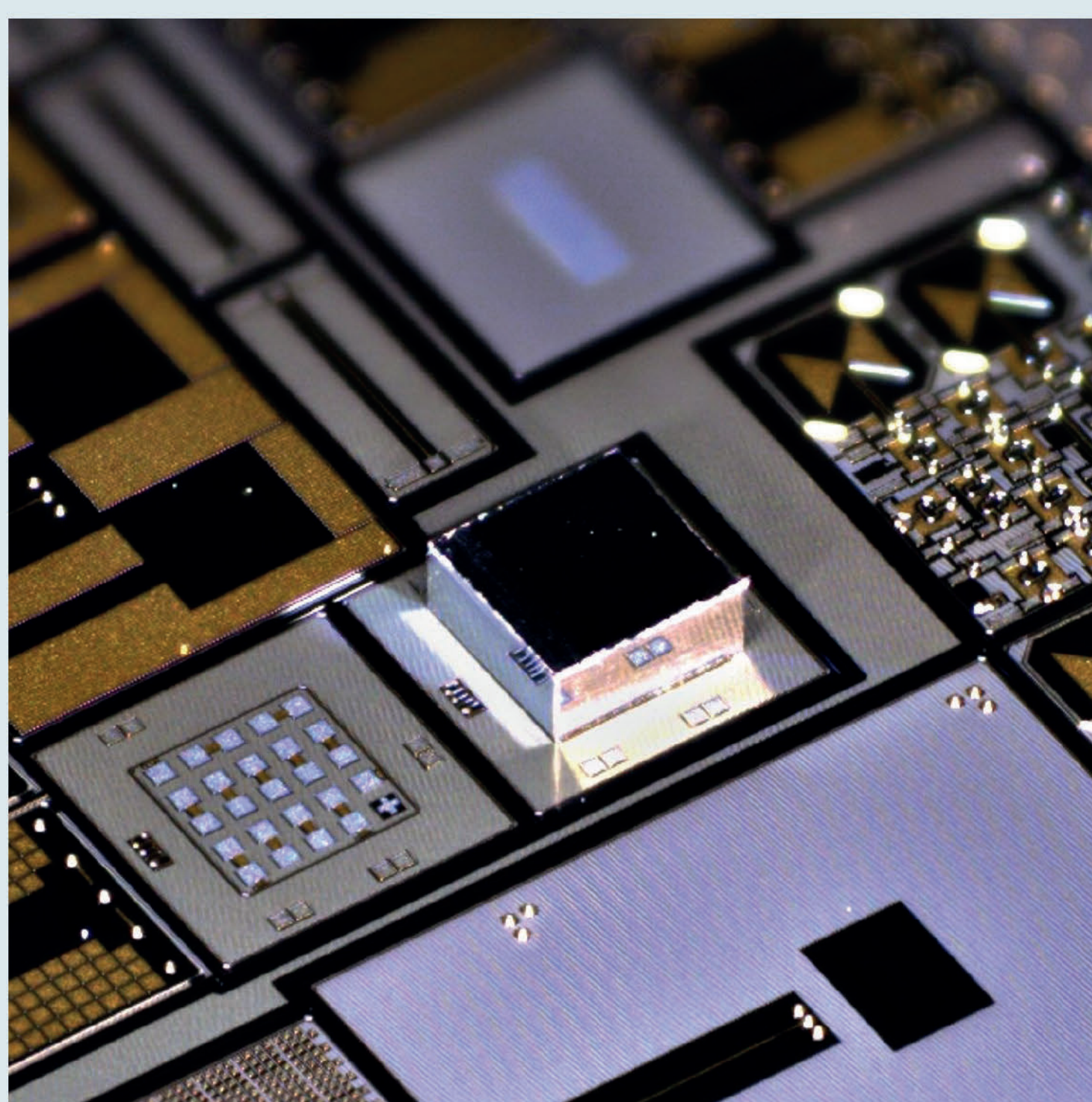
Within APECS, Leibniz IHP is establishing advanced BiCMOS wafer-level packaging platforms for mm-wave and sub-THz applications. Building on its core competence in AI-to-AI bonding, it develops novel Collective Die-to-Wafer (CD2W) technologies for the high-density integration of chiplets in high-frequency applications. In addition, it creates specific design environments to support seamless chiplet design. The institute also operates an industrial 8-inch SiGe BiCMOS cleanroom, enabling the production of high-performance SiGe technologies for THz applications, mm-wave chiplets, THz ASICs and electronic-photonic integrated circuits.

Leibniz IHP is enabling high-performance chiplet integration within APECS by:

- Developing high-performance chiplet integration platforms using an AI-to-AI bonding technology
- Implementing a QMI (quasi-monolithic integration) chiplet platform for SiGe/CMOS and BiCMOS technologies
- Building μ TP for InP photonic chiplets as well as Si chiplets (including manufacturing processes for Si chiplets)
- Developing SiGe-BiCMOS and silicon interposers as chiplet integration platforms with InP-DHBT and InGaAs-mHEMT
- Creating seamless ADK and PDK environments for multi-technology chiplet integration in open-source toolchains

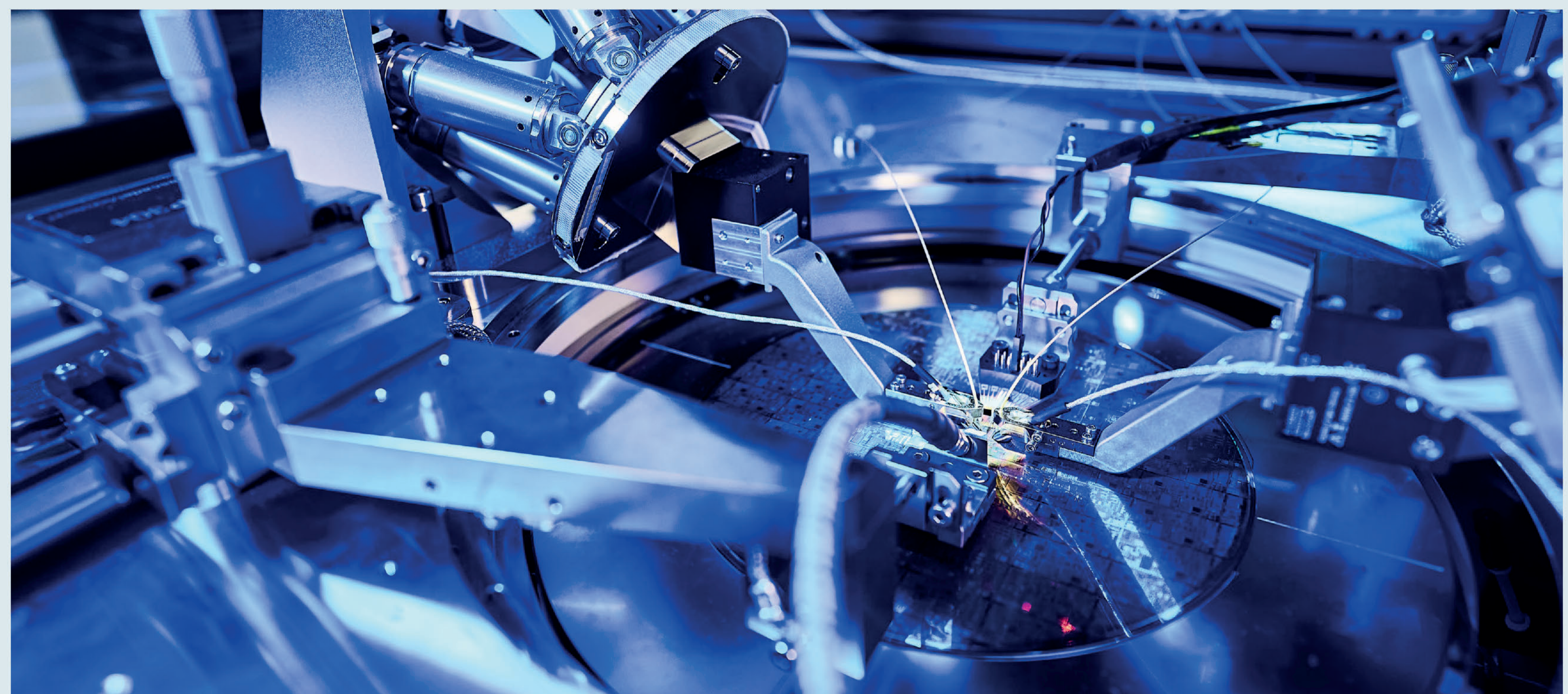
BiCMOS chiplet bonded to a silicon interposer using AI-to-AI bonding

© Leibniz IHP



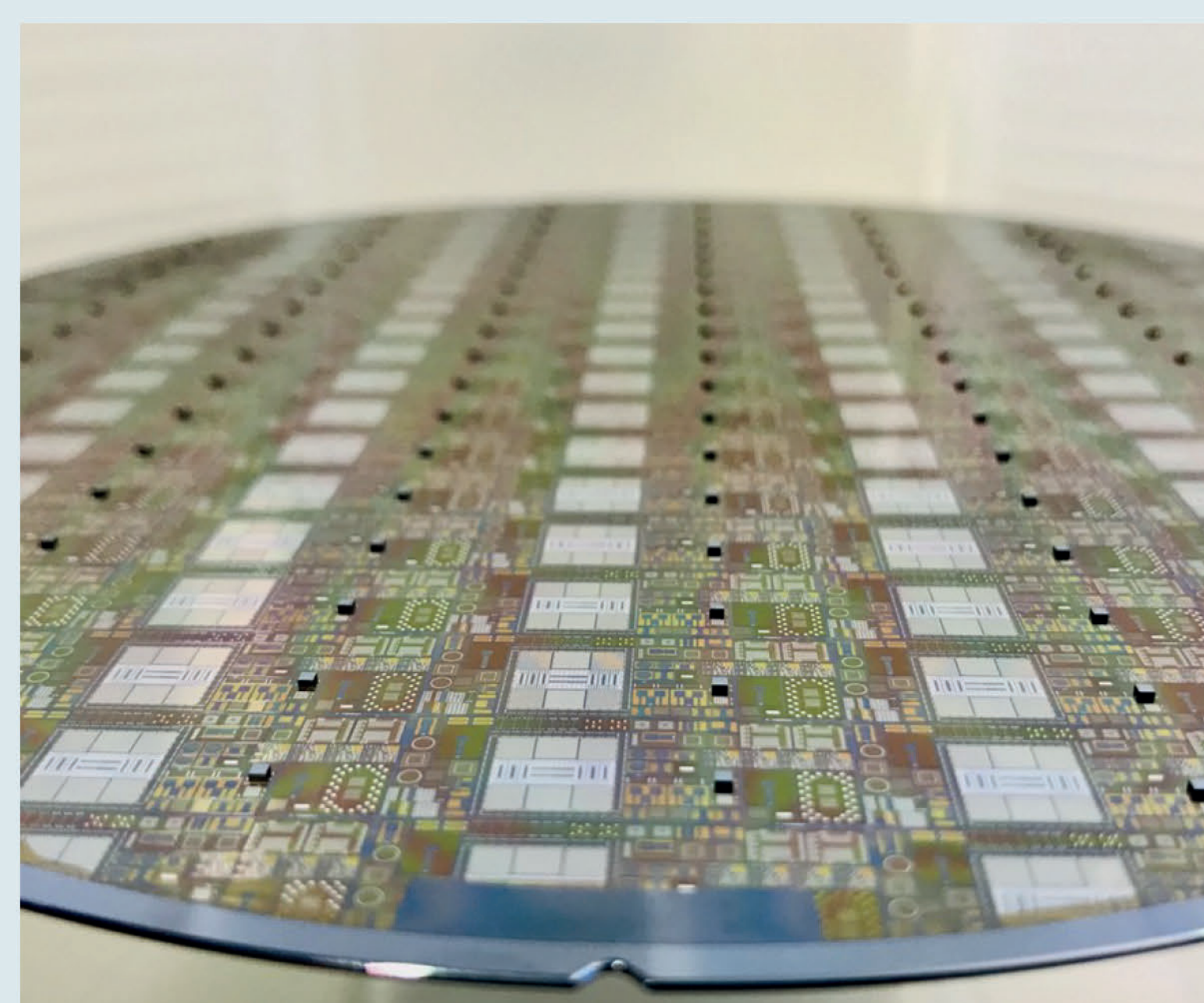
Electro-optical automated wafer probe platform for advanced IHP EPIC technologies

© Leibniz IHP



SiGe BiCMOS wafer with AI-to-AI bonded chiplets

© Leibniz IHP



Contributions to the APECS pilot line

Within APECS, IHP contributes its long-standing expertise in microelectronics research and helps connect fundamental research with application-oriented technology development.

IHP provides its SiGe chiplets for the RF and multi-material sensor demonstrators, and actively takes part in their planning and integration.

RF Demonstrator: 2.5D Heterointegration SiGe + InGaAs-on-Si

- SiGe BiCMOS + InGaAs-on-Si mHEMT on Si/Glass-Interposer
- IHP provides a H-band TRx radar chiplet and BEOL Si-Interposer

RF Demonstrator: 3D Heterointegration SiGe + InP

- SiGe BiCMOS + InP-DHBT by direct In-bump bonding
- IHP provides a 4-channel D-Band TRx chiplet

Multi-Material Sensor Demonstrator SiGe + Si-Opto

- SiGe BiCMOS + Si Opto-electronics on Si-Interposer with TSV
- IHP provides an ADC/iDAC chiplet with a temperature sensor

What is APECS?

APECS (Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems) is one of 5 European pilot lines established under the EU Chips Act. APECS is the foundation for Europe's competitive position in heterogeneous system integration and advanced packaging. It plays a vital role in enhancing Europe's strategic autonomy by reducing dependence on foreign suppliers and strengthening Europe's capabilities in critical technology areas.

Contact

Prof. Dr. Andreas Mai

Director of the Technology Department

IHP - Leibniz Institute for High Performance Microelectronics
Im Technologiepark 25
15236 Frankfurt (Oder)
Deutschland

Contact (Secretariat)

Phone : +49 335 5625 670
Email: Albani@ihp-microelectronics.com
www.apecs.eu | info@apecs.eu

Additional information

The work presented was carried out in the framework of the APECS Pilot Line of the Chips Joint Undertaking, funded by Horizon Europe and Digital Europe Programmes and national funding authorities of Austria, Belgium, Finland, France, Germany, Greece, Portugal, Spain.

Views and opinions expressed are however those of the author(s) only and do not necessarily reflect those of the European Union or the Chips Joint Undertaking. Neither the European Union nor the granting authority can be held responsible for them.